



Crimzon™ ZLR16300

***Z8 Low Voltage ROM MCUs
with Infrared Timers***

Product Specification

PS021410-0605



This publication is subject to replacement by a later edition. To determine whether a later edition exists, or to request copies of publications, contact:

ZiLOG Worldwide Headquarters

532 Race Street
San Jose, CA 95126-3432
Telephone: 408.558.8500
Fax: 408.558.8300
www.zilog.com

ZiLOG is a registered trademark of ZiLOG Inc. in the United States and in other countries. All other products and/or service names mentioned herein may be trademarks of the companies with which they are associated.

Document Disclaimer

©2005 by ZiLOG, Inc. All rights reserved. Information in this publication concerning the devices, applications, or technology described is intended to suggest possible uses and may be superseded. ZiLOG, INC. DOES NOT ASSUME LIABILITY FOR OR PROVIDE A REPRESENTATION OF ACCURACY OF THE INFORMATION, DEVICES, OR TECHNOLOGY DESCRIBED IN THIS DOCUMENT. ZiLOG ALSO DOES NOT ASSUME LIABILITY FOR INTELLECTUAL PROPERTY INFRINGEMENT RELATED IN ANY MANNER TO USE OF INFORMATION, DEVICES, OR TECHNOLOGY DESCRIBED HEREIN OR OTHERWISE. Devices sold by ZiLOG, Inc. are covered by warranty and limitation of liability provisions appearing in the ZiLOG, Inc. Terms and Conditions of Sale. ZiLOG, Inc. makes no warranty of merchantability or fitness for any purpose. Except with the express written approval of ZiLOG, use of information, devices, or technology as critical components of life support systems is not authorized. No licenses are conveyed, implicitly or otherwise, by this document under any intellectual property rights.



Revision History

Each instance in Table 1 reflects a change to this document from its previous revision. To see more detail, click the appropriate link in the table.

Table 1. Revision History of this Document

Date	Revision Level	Description	Page#
December 2004	07	Changed low power consumption and current usage for STOP and HALT modes, removed mask option note, and added characterization data to Table 7.	1, 2, 8
		Removed Preliminary designation	All
January 2005	08	Changed low power consumption value to 5mW. Changed STOP and HALT mode current values to 1.3μA and 0.5mA respectively. Changed V _{CC} Low Voltage Protection typical rating to 1.8V.	1, 12
April 2005	09	Clarified Port 1 reserved address status by removing Port 1 in Figure 1 and adding a note in Figure 12. Reference CR5843.	3, 21
June 2005	10	Added 1K and 2K parts.	All



Table of Contents

Revision History	iii
Features	1
General Description	2
Pin Description	5
Absolute Maximum Ratings	6
Standard Test Conditions	7
DC Characteristics	8
AC Characteristics	10
Pin Functions	12
XTAL1 Crystal 1 (Time-Based Input)	12
XTAL2 Crystal 2 (Time-Based Output)	12
Port 0 (P07–P00)	12
Port 2 (P27–P20)	13
Port 3 (P37–P30)	14
Functional Description	18
Program Memory	18
RAM	18
Expanded Register File	20
Register File	23
Stack	24
Timers	25
Counter/Timer Functional Blocks	33
Expanded Register File Control Registers (0D)	58
Expanded Register File Control Registers (0F)	63
Standard Control Registers	67
Package Information	73
Ordering Information	78



List of Figures

Figure 1. Functional Block Diagram	3
Figure 2. Counter/Timers Diagram	4
Figure 3. 20-Pin DIP/SOIC/SSOP Pin Configuration	5
Figure 4. 28-Pin DIP/SOIC/SSOP Pin Configuration	6
Figure 5. Test Load Diagram	7
Figure 6. AC Timing Diagram	10
Figure 7. Port 0 Configuration	13
Figure 8. Port 2 Configuration	14
Figure 9. Port 3 Configuration	15
Figure 10. Port 3 Counter/Timer Output Configuration	17
Figure 11. Program Memory Map	19
Figure 12. Expanded Register File Architecture	21
Figure 13. Register Pointer	22
Figure 14. Register Pointer—Detail	24
Figure 15. Glitch Filter Circuitry	33
Figure 16. Transmit Mode Flowchart	34
Figure 17. 8-Bit Counter/Timer Circuits	35
Figure 18. T8_OUT in Single-Pass Mode	36
Figure 19. T8_OUT in Modulo-N Mode	36
Figure 20. Demodulation Mode Count Capture Flowchart	37
Figure 21. Demodulation Mode Flowchart	38
Figure 22. 16-Bit Counter/Timer Circuits	39
Figure 23. T16_OUT in Single-Pass Mode	40
Figure 24. T16_OUT in Modulo-N Mode	40
Figure 25. Ping-Pong Mode Diagram	42
Figure 26. Output Circuit	42
Figure 27. Interrupt Block Diagram	44
Figure 28. Oscillator Configuration	46
Figure 29. Port Configuration Register (PCON) (Write Only)	48
Figure 30. Stop Mode Recovery Register	50
Figure 31. SCLK Circuit	51
Figure 32. Stop Mode Recovery Source	52
Figure 33. Stop Mode Recovery Register 2 ((0F) DH:D2–D4, D6 Write Only)	54



Figure 34. Watch-Dog Timer Mode Register (Write Only)	55
Figure 35. Resets and WDT	56
Figure 36. TC8 Control Register ((0D) 00H: Read/Write Except Where Noted)	59
Figure 37. T8 and T16 Common Control Functions ((0D) 01H: Read/Write)	60
Figure 38. T16 Control Register ((0D) 02H: Read/Write Except Where Noted)	61
Figure 39. T8/T16 control Register (0D) 03H: Read/Write (Except Where Noted)	62
Figure 40. Voltage Detection Register	63
Figure 41. Port Configuration Register (PCON) ((0F)00H: Write Only	64
Figure 42. Stop Mode Recovery Register ((0F) 0BH: D6–D0=Write Only, D7=Read Only)	65
Figure 43. Stop Mode Recovery Register 2 ((0F) 0DH: D2–D4, D6 Write Only)	66
Figure 44. Watch-Dog Timer Register ((0F) 0FH: Write Only)	67
Figure 45. Port 2 Mode Register (F6H: Write Only).....	67
Figure 46. Port 3 Mode Register (F7H: Write Only)	68
Figure 47. Port 0 Register (F8H: Write Only)	69
Figure 48. Interrupt Priority Register (F9H: Write Only)	70
Figure 49. Interrupt Request Register (FAH: Read/Write)	71
Figure 50. Interrupt Mask Register (FBH: Read/Write)	71
Figure 51. Flag Register (FCH: Read/Write)	72
Figure 52. Register Pointer (FDH: Read/Write)	72
Figure 53. Stack Pointer High (FEH: Read/Write)	73
Figure 54. Stack Pointer Low (FFH: Read/Write)	73
Figure 55. 20-Pin DIP Package Diagram	74
Figure 56. 20-Pin SOIC Package Diagram	74
Figure 57. 20-Pin SSOP Package Diagram	75
Figure 58. 28-Pin SOIC Package Diagram	76
Figure 59. 28-Pin DIP Package Diagram	77
Figure 60. 28-Pin SSOP Package Diagram	78



List of Tables

Table 1.	Revision History of this Document	iii
Table 2.	Features	1
Table 3.	Power Connections	2
Table 4.	20-Pin DIP/SOIC/SSOP Pin Identification	5
Table 5.	28-Pin DIP/SOIC/SSOP Pin Identification	6
Table 6.	Capacitance	8
Table 7.	DC Characteristics	8
Table 8.	AC Characteristics	11
Table 9.	Port 3 Pin Function Summary	16
Table 10.	CTR1(0D)01h T8 and T16 Common Functions	28
Table 11.	Interrupt Types, Sources, and Vectors	45
Table 12.	IRQ Register	45
Table 13.	SMR2(F)0DH:Stop Mode Recovery Register 2*	51
Table 14.	Stop Mode Recovery Source	53
Table 15.	Watch-Dog Timer Time Select	56
Table 16.	ROM Selectable Options	57



Features

Table 1 lists the features of ZiLOG®'s Crimzon™ ZLR16300 family members.

Table 1. Features

Device	ROM (KB)	RAM* (Bytes)	I/O Lines	Voltage Range
Crimzon™ ZLR16300	1, 2, 4, 8, 16	237	24, 16	2.0V–3.6V

* General purpose

- Low power consumption—5mW (typical)
- Three standby modes:
 - STOP—1.3μA (typical)
 - HALT—0.5mA (typical)
 - Low voltage reset
- Special architecture to automate both generation and reception of complex pulses or signals:
 - One programmable 8-bit counter/timer with two capture registers and two load registers
 - One programmable 16-bit counter/timer with one 16-bit capture register pair and one 16-bit load register pair
 - Programmable input glitch filter for pulse reception
- Six priority interrupts
 - Three external
 - Two assigned to counter/timers
 - One low-voltage detection interrupt
- Low voltage detection and high voltage detection flags
- Programmable Watch-Dog Timer (WDT)
- Power-On Reset (POR)
- Two independent comparators with programmable interrupt polarity
- Selectable pull-up transistors on ports 0, 2, 3

- Mask options
 - Port 0: 0–3 pull-ups
 - Port 0: 4–7 pull-ups
 - Port 2: 0–7 pull-ups
 - Port 3: 0–3 pull-ups
 - Watch-Dog Timer at Power On Reset

General Description

The Crimzon™ ZLR16300 is a ROM-based member of the MCU family of general purpose microcontrollers. With 1KB to 16KB of program memory and 237B of general purpose RAM, ZiLOG®'s CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The Crimzon™ ZLR16300 architecture (Figures 1 and 2) is based on ZiLOG®'s 8-bit microcontroller core with an Expanded Register File allowing access to register-mapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8® core offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

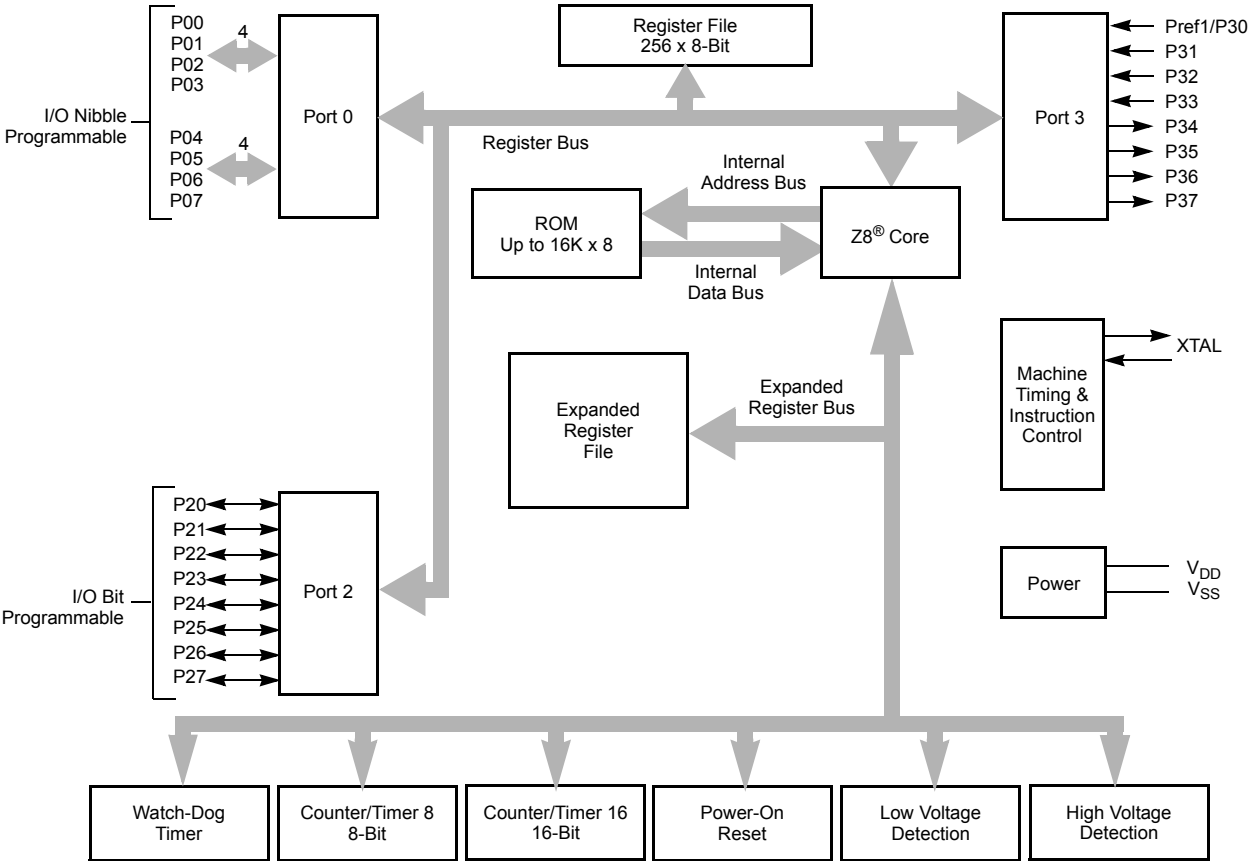
There are three basic address spaces available to support a wide range of configurations: Program Memory, Register File and Expanded Register File. The register file is composed of 256B of RAM. It includes three I/O port registers, 16 control and status registers, and 237 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Crimzon™ ZLR16300 offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see Figure 2). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages.

Power connections use the conventional descriptions listed in Table 2.

Table 2. Power Connections

Connection	Circuit	Device
Power	V _{CC}	V _{DD}
Ground	GND	V _{SS}



Note: Refer to the specific package for available pins.

Figure 1. Functional Block Diagram

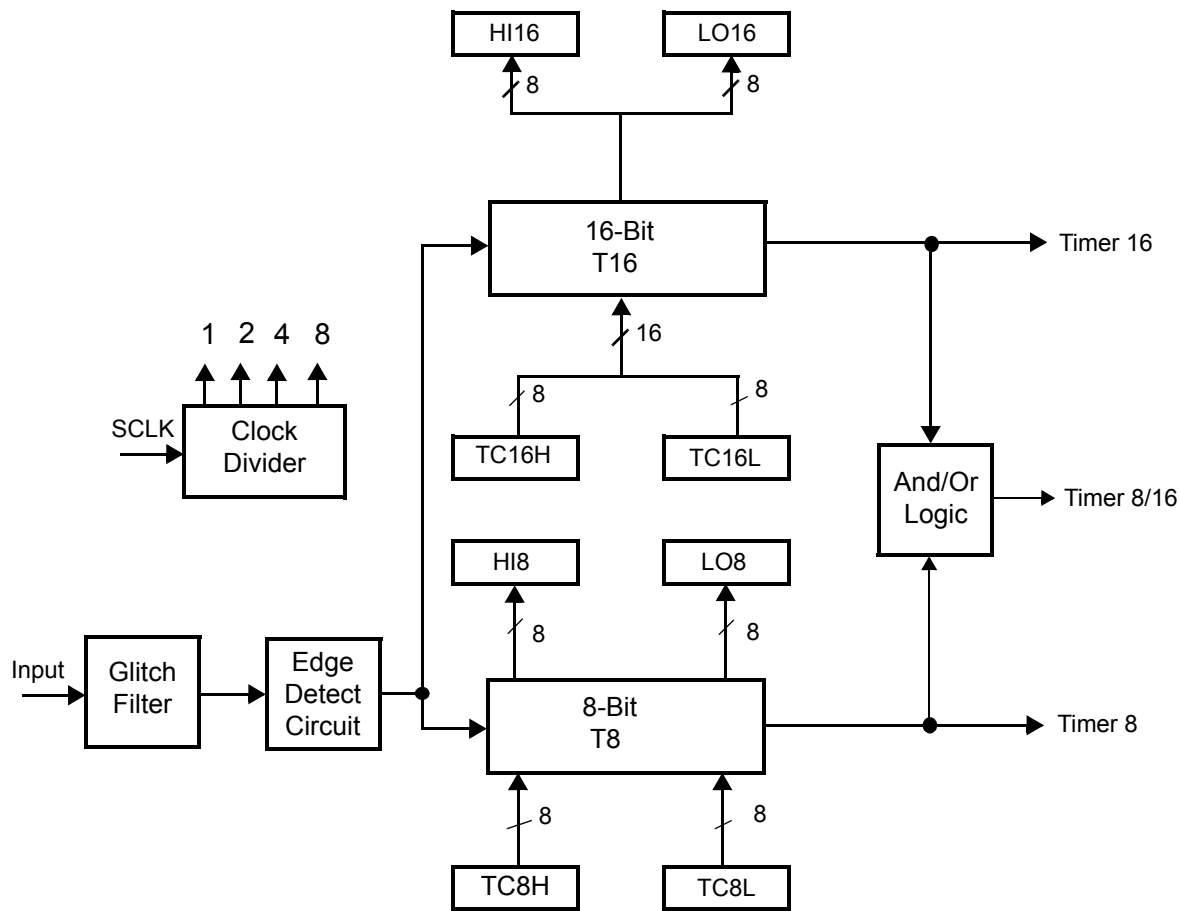


Figure 2. Counter/Timers Diagram

Pin Description

The pin configuration for the 20-pin DIP/SOIC/SSOP is illustrated in Figure 3 and described in Table 3. The pin configuration for the 28-pin DIP/SOIC/SSOP are depicted in Figure 4 and described in Table 4.

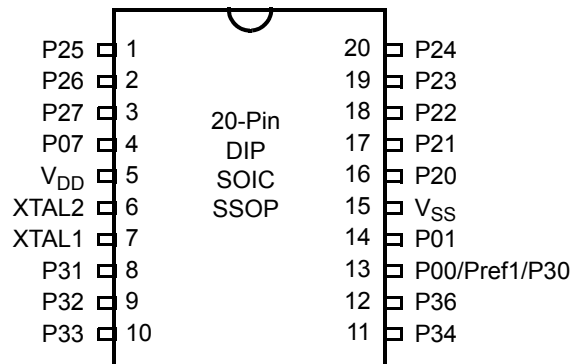


Figure 3. 20-Pin DIP/SOIC/SSOP Pin Configuration

Table 3. 20-Pin DIP/SOIC/SSOP Pin Identification

Pin #	Symbol	Function	Direction
1–3	P25–P27	Port 2, Bits 5,6,7	Input/Output
4	P07	Port 0, Bit 7	Input/Output
5	V _{DD}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8–10	P31–P33	Port 3, Bits 1,2,3	Input
11,12	P34, P36	Port 3, Bits 4,6	Output
13	P00/Pref1/P30	Port 0, Bit 0/Analog reference input Port 3, Bit 0	Input/Output for P00 Input for Pref1/P30
14	P01	Port 0, Bit 1	Input/Output
15	V _{SS}	Ground	
16–20	P20–P24	Port 2, Bits 0,1,2,3,4	Input/Output

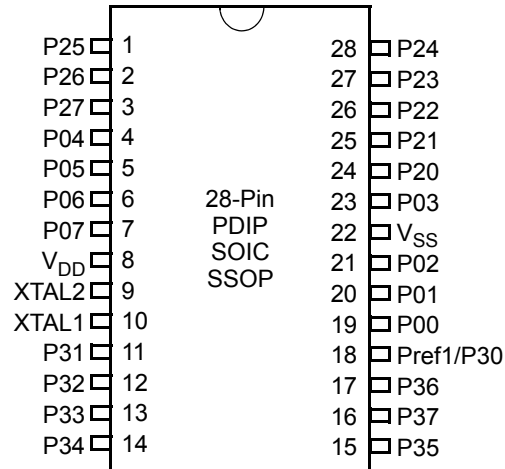


Figure 4. 28-Pin DIP/SOIC/SSOP Pin Configuration

Table 4. 28-Pin DIP/SOIC/SSOP Pin Identification

Pin	Symbol	Direction	Description
1-3	P25-P27	Input/Output	Port 2, Bits 5,6,7
4-7	P04-P07	Input/Output	Port 0, Bits 4,5,6,7
8	V _{DD}		Power supply
9	XTAL2	Output	Crystal, oscillator clock
10	XTAL1	Input	Crystal, oscillator clock
11-13	P31-P33	Input	Port 3, Bits 1,2,3
14	P34	Output	Port 3, Bit 4
15	P35	Output	Port 3, Bit 5
16	P37	Output	Port 3, Bit 7
17	P36	Output	Port 3, Bit 6
18	Pref1	Input	Analog ref input; connect to V _{CC} if not used Port 3 Bit 0
19-21	P00-P02	Input/Output	Port 0, Bits 0,1,2
22	V _{SS}		Ground
23	P03	Input/Output	Port 0, Bit 3
24-28	P20-P24	Input/Output	Port 2, Bits 0-4

Absolute Maximum Ratings

Stresses greater than those listed in Table 5 might cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at

any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period might affect device reliability.

Table 5. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units	Notes
Ambient temperature under bias	0	+70	C	
Storage temperature	−65	+150	C	
Voltage on any pin with respect to V_{SS}	−0.3	+4.0	V	1
Voltage on V_{DD} pin with respect to V_{SS}	−0.3	+3.6	V	
Maximum current on input and/or inactive output pin	−5	+5	mA	
Maximum output current from active output pin	−25	+25	mA	
Maximum current into V_{DD} or out of V_{SS}		75	mA	

Note:

1. This voltage applies to all pins except the following: V_{DD} .

Standard Test Conditions

The characteristics listed in this product specification apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 5).

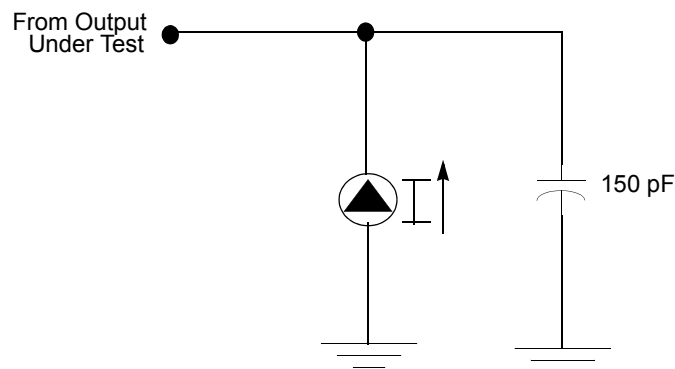


Figure 5. Test Load Diagram

Capacitance

Table 6 lists the capacitances.

Table 6. Capacitance

Parameter	Maximum
Input capacitance	12pF
Output capacitance	12pF
I/O capacitance	12pF
Note: $T_A = 25^\circ\text{C}$, $V_{CC} = \text{GND} = 0\text{ V}$, $f = 1.0\text{ MHz}$, unmeasured pins returned to GND	

DC Characteristics

Table 7. DC Characteristics

Symbol	Parameter	V_{CC}	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$			Units	Conditions	Notes
			Min	Typ(7)	Max			
V_{CC}	Supply Voltage		2.0 V		3.6	V	See Note 5	
V_{CH}	Clock Input High Voltage	2.0-3.6V	$0.8 V_{CC}$		$V_{CC}+0.3$	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.0-3.6V	$V_{SS}-0.3$		0.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0-3.6V	$0.7 V_{CC}$		$V_{CC}+0.3$	V		
V_{IL}	Input Low Voltage	2.0-3.6V	$V_{SS}-0.3$		$0.2 V_{CC}$	V		
V_{OH1}	Output High Voltage	2.0-3.6V	$V_{CC}-0.4$			V	$I_{OH} = -0.5\text{mA}$	
V_{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-3.6V	$V_{CC}-0.8$			V	$I_{OH} = -7\text{mA}$	
V_{OL1}	Output Low Voltage	2.0-3.6V			0.4	V	$I_{OL} = 4.0\text{mA}$	
V_{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-3.6V			0.8	V	$I_{OL} = 10\text{mA}$	
V_{OFFSET}	Comparator Input Offset Voltage	2.0-3.6V			25	mV		
V_{REF}	Comparator Reference Voltage	2.0-3.6V	0		V_{DD} -1.75	V		
I_{IL}	Input Leakage	2.0-3.6V	-1		1	μA	$V_{IN} = 0\text{V}$, V_{CC} Pull-ups disabled	
R_{PU}	Pull-up Resistance	2.0V	225		675	$\text{K}\Omega$	$V_{IN} = 0\text{V}$; Pullups selected by mask option	
		3.6V	75		275	$\text{K}\Omega$		
I_{OL}	Output Leakage	2.0-3.6V	-1		1	μA	$V_{IN} = 0\text{V}$, V_{CC}	
I_{CC}	Supply Current	2.0 V		1.2	3	mA	at 8.0MHz	1, 2
		3.6 V		2.1	5	mA	at 8.0MHz	1, 2



Table 7. DC Characteristics (Continued)

Symbol	Parameter	V _{CC}	T _A = 0°C to +70°C			Units	Conditions	Notes
			Min	Typ(7)	Max			
I _{CC1}	Standby Current (HALT Mode)	2.0 V		0.5	1.6	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6
		3.6 V		0.8	2.0	mA	Same as above	1, 2, 6
I _{CC2}	Standby Current (STOP Mode)	2.0 V		1.2	8	μA	V _{IN} = 0 V, V _{CC} WDT is not Running	3
		3.6 V		1.4	10	μA	Same as above	3
		2.0 V		3.5	20	μA	V _{IN} = 0 V, V _{CC} WDT is Running	3
		3.6 V		6.5	30	μA	Same as above	3
I _{LV}	Standby Current (Low Voltage)			0.8	6	μA	Measured at 1.3V	4
V _{BO}	V _{CC} Low Voltage Protection			1.8	2.0	V	8MHz maximum Ext. CLK Freq.	
V _{LVD}	V _{CC} Low Voltage Detection			2.4		V		
V _{HVD}	V _{CC} High Voltage Detection			2.7		V		

Notes:

1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. Oscillator stopped.
4. Oscillator stops when V_{CC} falls below V_{BO} limit.
5. It is strongly recommended to add a filter capacitor (minimum 0.1 μF), physically close to VDD and V_{SS} pins if operating voltage fluctuations are anticipated, such as those resulting from driving an IR LED.
6. Comparators and Timers are on. Interrupt disabled.
7. Typical values shown are at 25 degrees C.



AC Characteristics

Figure 6 and Table 8 describe the Alternating Current (AC) characteristics.

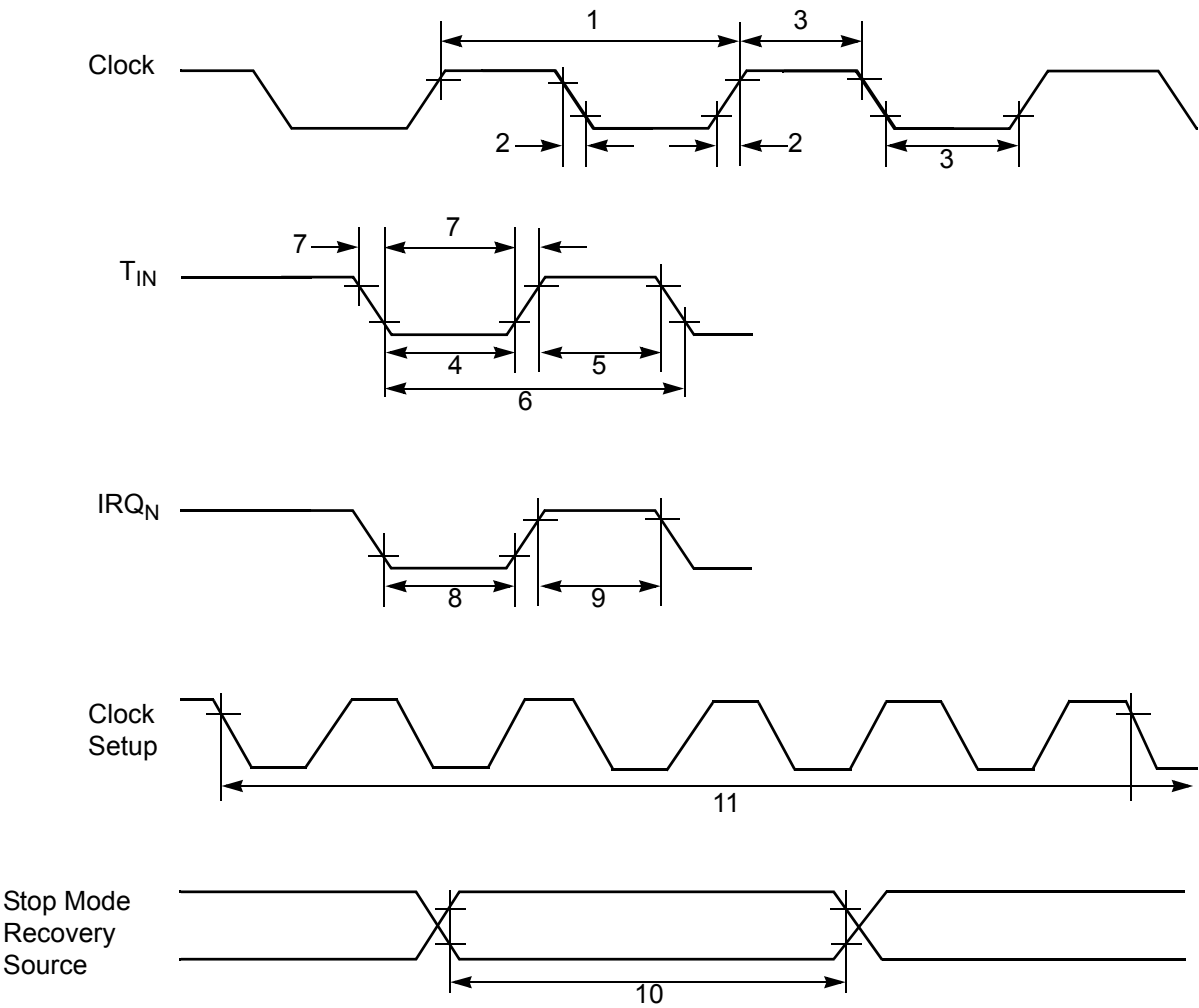


Figure 6. AC Timing Diagram



Table 8. AC Characteristics

T _A =0°C to +70°C 8.0MHz							Watch-Dog Timer Mode Register (D1, D0)
No	Symbol	Parameter	V _{CC}	Minimum	Maximum	Units	Notes
1	TpC	Input Clock Period	2.0–3.6	121	DC	ns	1
2	TrC, TfC	Clock Input Rise and Fall Times	2.0–3.6		25	ns	1
3	TwC	Input Clock Width	2.0–3.6	37		ns	1
4	TwTinL	Timer Input Low Width	2.0 3.6	100 70		ns	1
5	TwTinH	Timer Input High Width	2.0–3.6	3TpC			1
6	TpTin	Timer Input Period	2.0–3.6	8TpC			1
7	TrTin, TfTin	Timer Input Rise and Fall Timers	2.0–3.6		100	ns	1
8	TwIL	Interrupt Request Low Time	2.0 3.6	100 70		ns	1, 2
9	TwIH	Interrupt Request Input High Time	2.0–3.6	10TpC			1, 2
10	Twsm	Stop-Mode Recovery Width Spec	2.0–3.6	12 10TpC		ns	3 4
11	Tost	Oscillator Start-Up Time	2.0–3.6		5TpC		4
12	Twdt	Watch-Dog Timer Delay Time	2.0–3.6 2.0–3.6 2.0–3.6 2.0–3.6	10 20 40 160		ms ms ms ms	0, 0 0, 1 1, 0 1, 1
13	T _{POR}	Power-On Reset	2.0–3.6	2.5	10	ms	

Notes:

1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. SMR – D5 = 1.
4. SMR – D5 = 0.



Pin Functions

XTAL1 Crystal 1 (Time-Based Input)

This pin connects a parallel-resonant crystal or ceramic resonator to the on-chip oscillator input. Additionally, an external single-phase clock can be connected to the on-chip oscillator input.

XTAL2 Crystal 2 (Time-Based Output)

This pin connects a parallel-resonant crystal or ceramic resonant to the on-chip oscillator output.

Port 0 (P07–P00)

Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port. The output drivers are push-pull or open-drain controlled by bit D2 in the PCON register.

If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. After a hardware reset, Port 0 is configured (Figure 7) as an input port.

An optional pull-up transistor is available as a mask option on all Port 0 bits with nibble select.

- **Notes:** Internal pull-ups are disabled on any given pin or group of port pins when programmed into Output mode.

The Port 0 direction is reset to be input following an SMR.

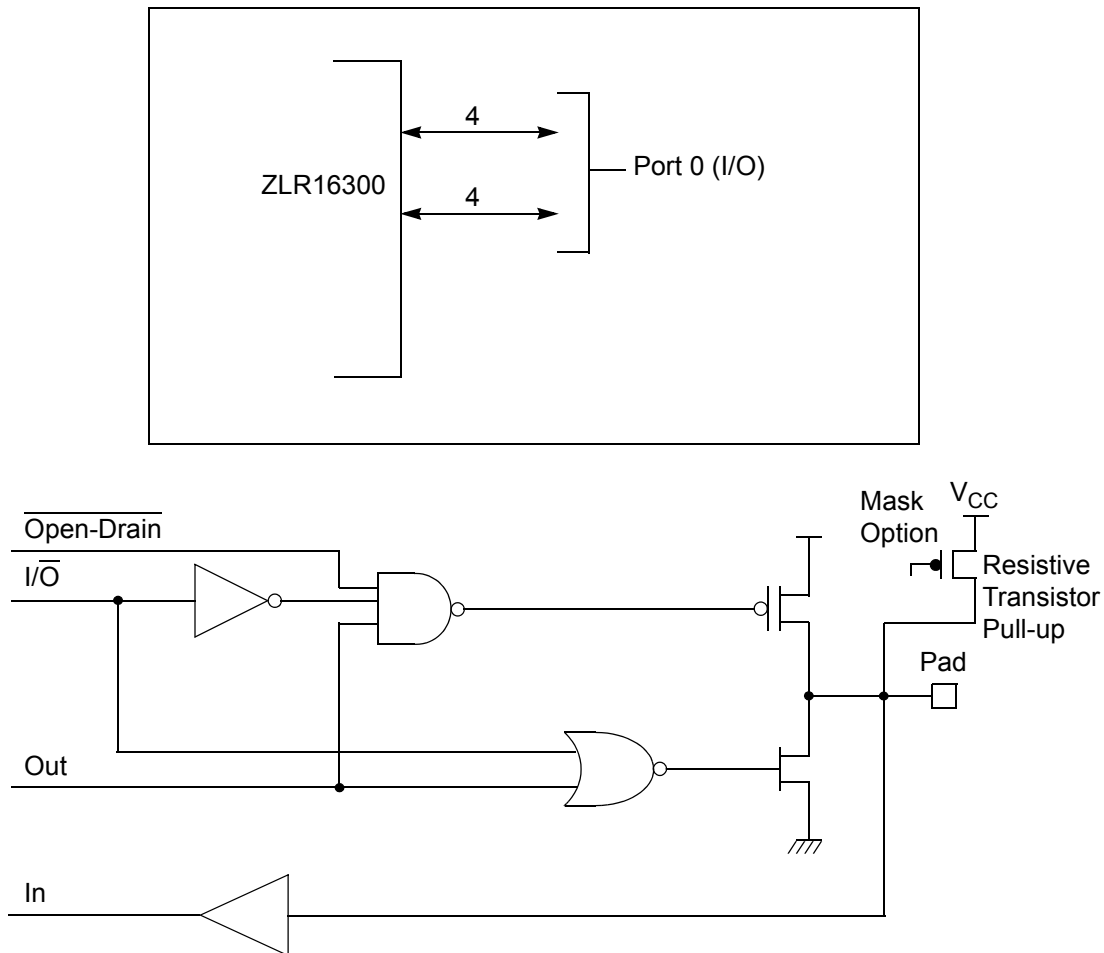


Figure 7. Port 0 Configuration

Port 2 (P27–P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see Figure 8). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A mask option is available to connect eight pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. The POR resets with the eight bits of Port 2 configured as inputs.

Port 2 also has an 8-bit input OR and AND gate, which can be used to wake up the part. P20 can be programmed to access the edge-detection circuitry in Demodulation mode.

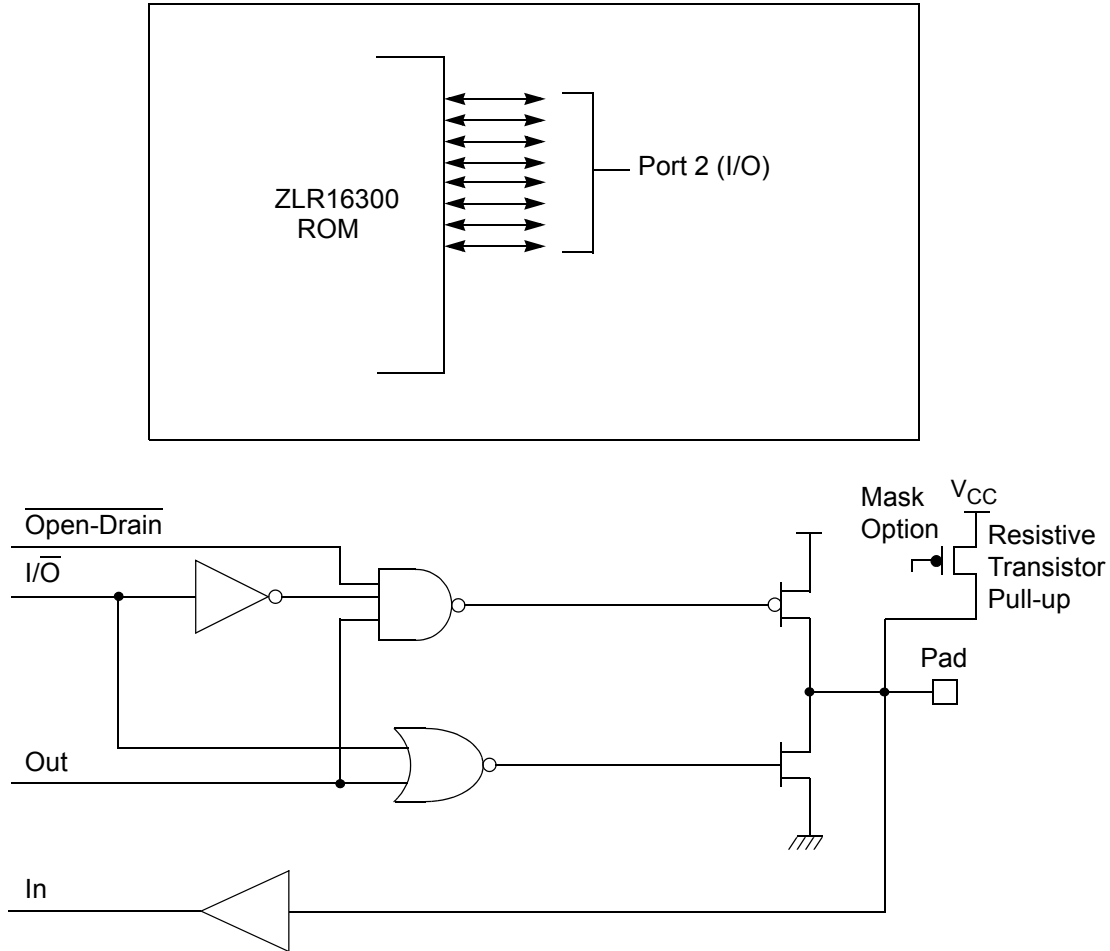


Figure 8. Port 2 Configuration

Port 3 (P37–P30)

Port 3 is an 8-bit, CMOS-compatible fixed I/O port (see Figure 9). Port 3 consists of four fixed input (P33–P30) and four fixed output (P37–P34), which can be configured under software control for interrupt and as output from the counter/timers. P30, P31, P32, and P33 are standard CMOS inputs; P34, P35, P36, and P37 are push-pull outputs.

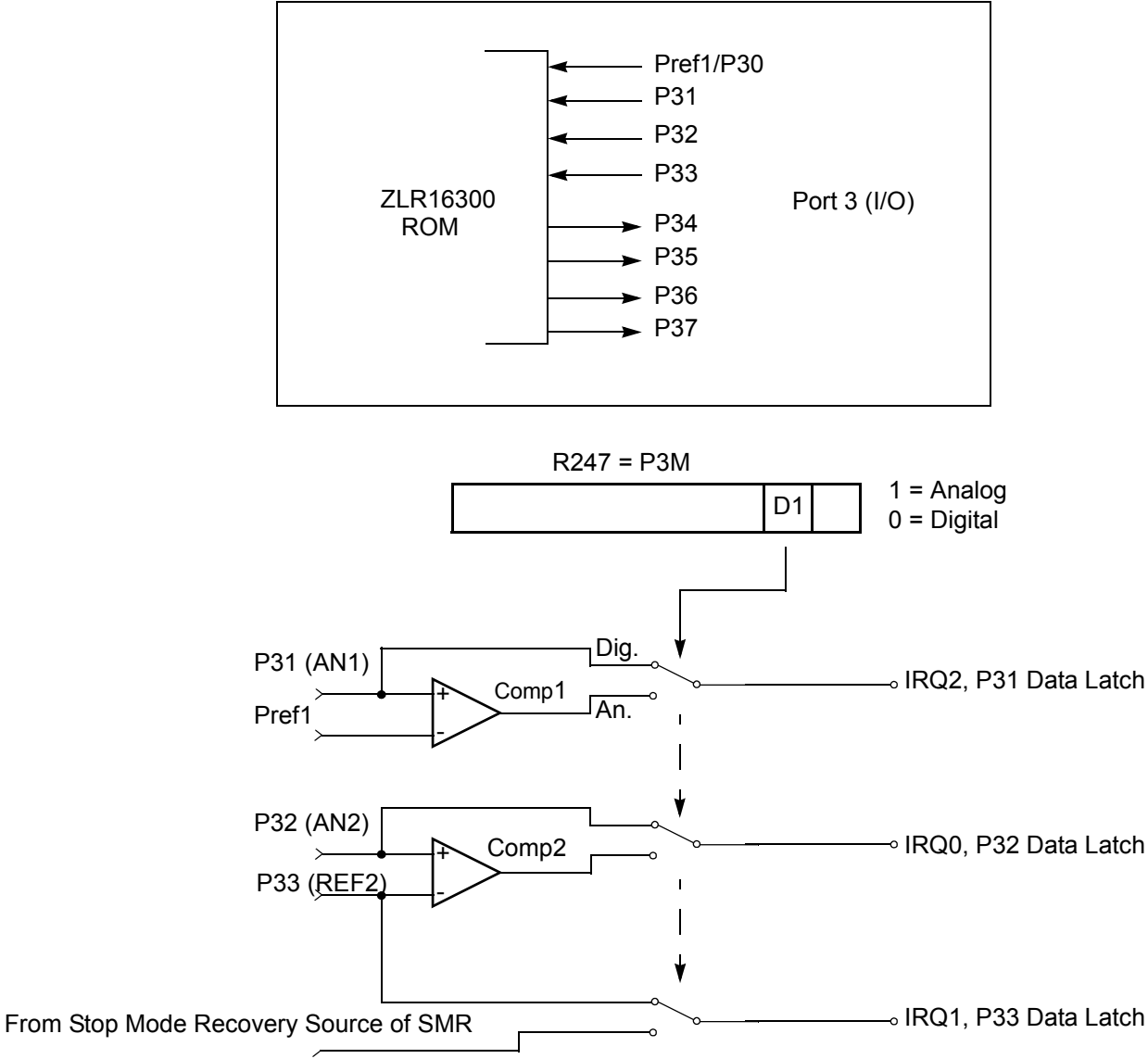


Figure 9. Port 3 Configuration

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edge-detection circuit is through P31 or P20 (see “T8 and T16 Common Functions—“T8



and T16 Common Functions—CTR1(0D)01h” on page 28). Other edge detect and IRQ modes are described in Table 9.

- **Note:** Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery (SMR) source, these inputs must be placed into Digital mode.

²
Table 9. Port 3 Pin Function Summary

Pin	I/O	Counter/Timers	Comparator	Interrupt
Pref1/P30	IN		RF1	
P31	IN	IN	AN1	IRQ2
P32	IN		AN2	IRQ0
P33	IN		RF2	IRQ1
P34	OUT	T8	AO1	
P35	OUT	T16		
P36	OUT	T8/16		
P37	OUT		AO2	
P20	I/O	IN		

Port 3 also provides output for each of the counter/timers and the AND/OR Logic (see Figure 10). Control is performed by programming bits D5–D4 of CTR1, bit 0 of CTR0, and bit 0 of CTR2.

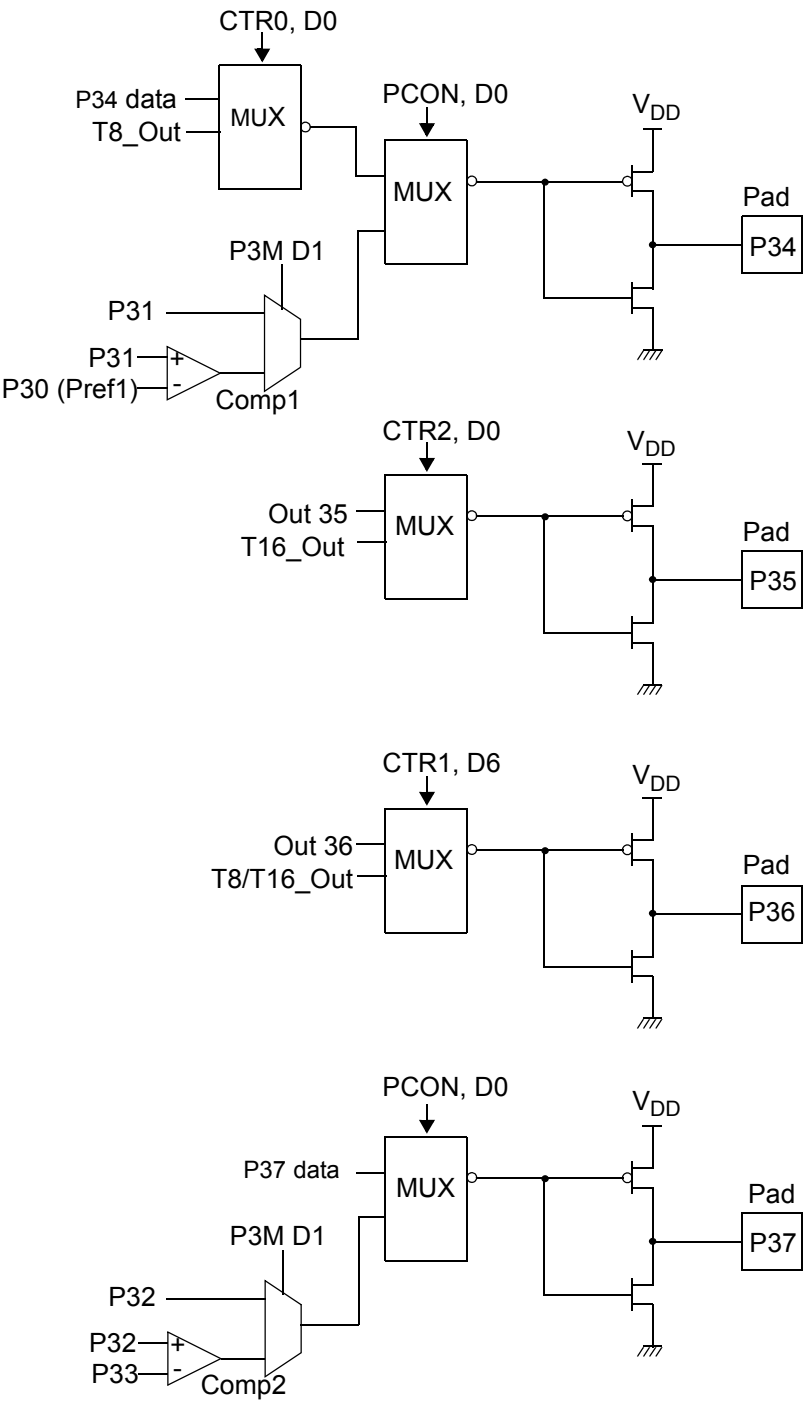


Figure 10. Port 3 Counter/Timer Output Configuration



Comparator Inputs

In ANALOG mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as indicated in Figure 9 on page 15. In digital mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.

- **Note:** Comparators are powered down by entering STOP mode. For P31–P33 to be used in a STOP Mode Recovery source, these inputs must be placed into Digital mode.

Comparator Outputs

These channels can be programmed to be output on P34 and P37 through the PCON register.

Functional Description

These devices incorporate special functions to enhance the Z8®'s functionality in consumer and battery-operated applications.

Program Memory

These devices address from 1KB to 16KB of program memory. The first 12 Bytes are reserved for interrupt vectors. These locations contain the six 16-bit vectors that correspond to the six available interrupts. See Figure 11.

RAM

The ZLR16300 product family features 237 Bytes of RAM.

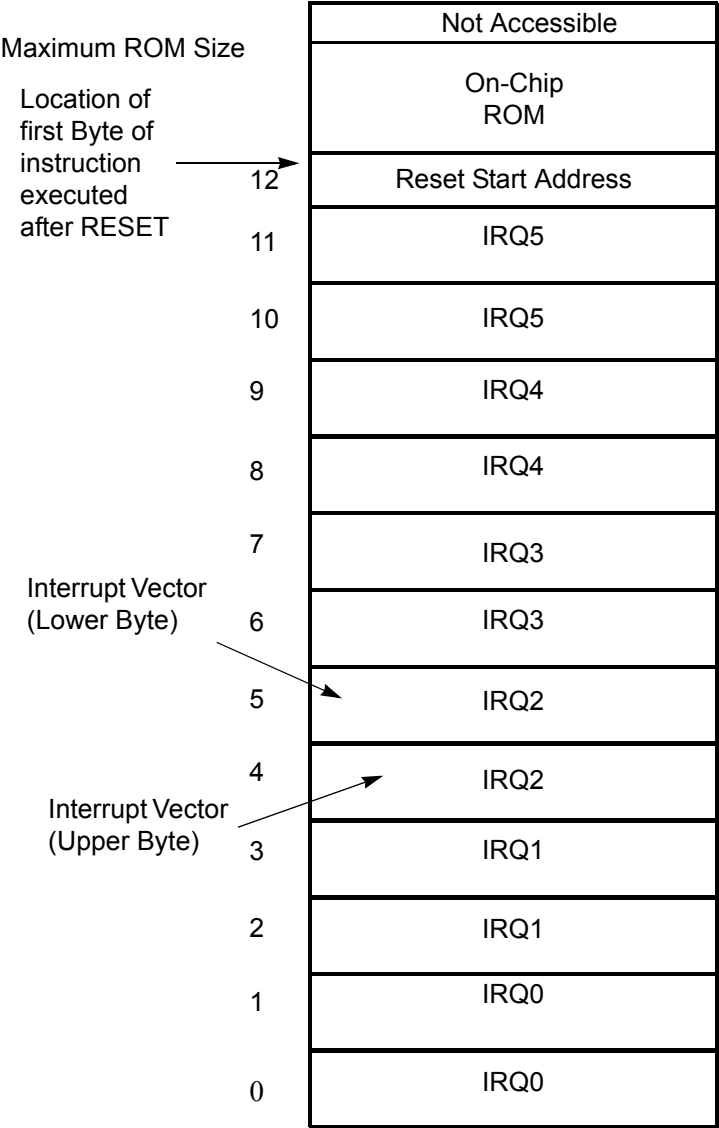


Figure 11. Program Memory Map



Expanded Register File

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The Z8® register address space (0 through 15 (0Fh)) has been implemented as 16 banks, with 16 registers per bank. These register banks are known as the ERF (Expanded Register File). Bits 7–4 of register RP select the working register group. Bits 3–0 of register RP select the expanded register file bank.

- **Note:** An expanded register bank is also referred to as an expanded register group (see Figure 12).



The upper nibble of the register pointer (see Figure 13) selects which working register group, of 16 bytes in the register file, is accessed out of the possible 256. The lower nibble selects the expanded register file bank and in the case of the Crimzon™ ZLR16300 family, banks 0, F, and D are implemented. A 0h in the lower nibble allows the normal register file (bank 0) to be addressed. Any other value from 1h to Fh exchanges the lower 16 registers to the selected expanded register bank.

R253 RP

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

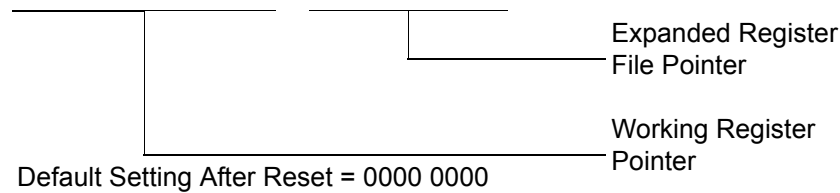


Figure 13. Register Pointer

Example: (See Figure 12 on page 21)

R253 RP = 00h

R0 = Port 0

R2 = Port 2

R3 = Port 3

But if:

R253 RP = 0Dh

R0 = CTR0

R1 = CTR1

R2 = CTR2

R3 = CTR3

The counter/timers are mapped into ERF group D. Access is easily performed using the following:

```
LD                                RP, #0Dh                ;Select ERF D for
                                ;access to bank D
                                ;(working register
group 0)
LD                                R0, #xx                ;load CTR0
LD                                1, #xx                 ;load CTR1
LD                                R1, 2                  ;CTR2→CTR1

LD                                RP, #0Dh                ;Select ERF D for
                                ;access to bank D
                                ; (working register
group 0)
LD                                RP, #7Dh                ;Select expanded
register bank D and working      ;register group 7 of
bank 0 for access.
LD                                71h, 2                  ;CTRL2→register 71h
LD                                R1, 2                  ;CTRL2→register 71h
```

Register File

The register file (bank 0) consists of 3 I/O port registers, 237 general-purpose registers, 16 control and status registers (R0, R2, R3, R4–R239, and R240–R255, respectively), and two expanded register Banks D (see Table 10) and F. Instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing a short, 4-bit register address to use the Register Pointer (Figure 14). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

- **Note:** Register address E0h–EFh can only be accessed through working registers and indirect addressing modes.

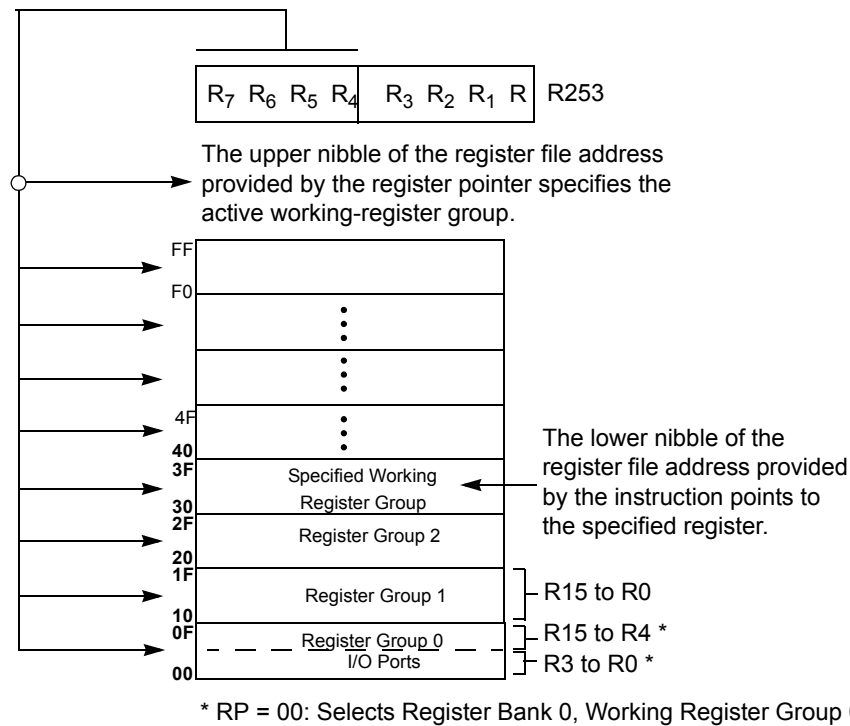


Figure 14. Register Pointer—Detail

Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.

Timers

T8_Capture_HI—HI8(0D)0Bh

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 1.

Field	Bit Position	Description
T8_Capture_HI	[7:0]	R/W Captured Data - No Effect

T8_Capture_LO—L08(0D)0Ah

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 0.

Field	Bit Position	Description
T8_Capture_LO	[7:0]	R/W Captured Data - No Effect

T16_Capture_HI—HI16(0D)09h

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

Field	Bit Position	Description
T16_Capture_HI	[7:0]	R/W Captured Data - No Effect

T16_Capture_LO—L016(0D)08h

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

Field	Bit Position	Description
T16_Capture_LO	[7:0]	R/W Captured Data - No Effect

Counter/Timer2 MS-Byte Hold Register—TC16H(0D)07h

Field	Bit Position	Description
T16_Data_HI	[7:0]	R/W Data

Counter/Timer2 LS-Byte Hold Register—TC16L(0D)06h

Field	Bit Position	Description
T16_Data_LO	[7:0]	R/W Data

Counter/Timer8 High Hold Register—TC8H0(D)05h

Field	Bit Position	Description
T8_Level_HI	[7:0]	R/W Data

Counter/Timer8 Low Hold Register—TC8L(0D)04h

Field	Bit Position	Description
T8_Level_LO	[7:0]	R/W Data

CTR0 Counter/Timer8 Control Register—CTR0(0D)00h

Table 10 lists and briefly describes the fields for this register.

Table 10. CTR0(0D)00h Counter/Timer8 Control Register

Field	Bit Position		Value	Description
T8_Enable	7-----	R/W	0*	Counter Disabled
			1	Counter Enabled
			0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6-----	R/W	0*	Modulo-N
			1	Single Pass
Time_Out	--5-----	R/W	0**	No Counter Time-Out
			1	Counter Time-Out Occurred
			0	No Effect
			1	Reset Flag to 0
T8_Clock	---43---	R/W	0 0**	SCLK
			0 1	SCLK/2
			1 0	SCLK/4
			1 1	SCLK/8
Capture_INT_Mask	----2--	R/W	0**	Disable Data Capture Interrupt
			1	Enable Data Capture Interrupt

Table 10. CTR0(0D)00h Counter/Timer8 Control Register (Continued)

Field	Bit Position		Value	Description
Counter_INT_Mask	-----1-	R/W	0**	Disable Time-Out Interrupt
			1	Enable Time-Out Interrupt
P34_Out	-----0	R/W	0*	P34 as Port Output
			1	T8 Output on P34

Note:

*Indicates the value at Power-On Reset.

** Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

T8 Enable

This field enables T8 when set (written) to 1.

Single/Modulo-N

When set to 0 (Modulo-N), the counter reloads the initial value when the terminal count is reached. When set to 1 (Single-Pass), the counter stops when the terminal count is reached.

Timeout

This bit is set when T8 times out (terminal count reached). To reset this bit, write a 1 to its location.



Caution: Writing a 1 is the only way to reset the Terminal Count status condition. Reset this bit before using/enabling the counter/timers.

The first clock of T8 might not have complete clock width and can occur any time when enabled.



Note: Take care when using the OR or AND commands to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (Demodulation Mode). These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers is ORed or ANDed with the designated value and then written back into the registers.

T8 Clock

These bits define the frequency of the input signal to T8.

**Capture_INT_Mask**

Set this bit to allow an interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in Capture Mode.

Counter_INT_Mask

Set this bit to allow an interrupt when T8 has a timeout.

P34_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

T8 and T16 Common Functions—CTR1(0D)01h

This register controls the functions in common with the T8 and T16.

Table 11 lists and briefly describes the fields for this register.

Table 11. CTR1(0D)01h T8 and T16 Common Functions

Field	Bit Position		Value	Description
Mode	7-----	R/W	0*	Transmit Mode
			1	Demodulation Mode
P36_Out/ Capture_Input	-6-----	R/W	0*	Transmit Mode
			1	Port Output
			0*	T8/T16 Output
			1	Demodulation Mode
T8/T16_Logic/ Edge_Detect	--54----	R/W	0*	P31
			1	P20
			00**	Transmit Mode
			01	AND
			10	OR
			11	NOR
			00**	NAND
			01	Demodulation Mode
			00**	Falling Edge
			01	Rising Edge
			10	Both Edges
			11	Reserved



Table 11. CTR1(0D)01h T8 and T16 Common Functions (Continued)

Field	Bit Position		Value	Description
Transmit_Submode/ Glitch_Filter	----32--	R/W	00	Transmit Mode
			01	Normal Operation
			10	Ping-Pong Mode
			11	T16_Out = 0
			11	T16_Out = 1
			00	Demodulation Mode
			01	No Filter
			10	4 SCLK Cycle
			11	8 SCLK Cycle
			11	Reserved
Initial_T8_Out/ Rising Edge	-----1-	R/W	0	Transmit Mode
			1	T8_OUT is 0 Initially
		R	0	T8_OUT is 1 Initially
			1	Demodulation Mode
		W	0	No Rising Edge
			1	Rising Edge Detected
			0	No Effect
			1	Reset Flag to 0
Initial_T16_Out/ Falling_Edge	-----0	R/W	0	Transmit Mode
			1	T16_OUT is 0 Initially
		R	0	T16_OUT is 1 Initially
			1	Demodulation Mode
		W	0	No Falling Edge
			1	Falling Edge Detected
			0	No Effect
			1	Reset Flag to 0

Note:

*Default at Power-On Reset.

** Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

Mode

If the result is 0, the counter/timers are in Transmit mode; otherwise, they are in Demodulation Mode.

P36_Out/Demodulator_Input

In Transmit Mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In Demodulation Mode, this bit defines whether the input signal to the Counter/Timers is from P20 or P31.



If the input signal is from Port 31, a capture event may also generate an IRQ2 interrupt. To prevent generating an IRQ2, either disable the IRQ2 interrupt by clearing its IMR bit D2 or use P20 as the input.

T8/T16_Logic/Edge_Detect

In Transmit Mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In Demodulation Mode, this field defines which edge should be detected by the edge detector.

Transmit_Submode/Glitch Filter

In Transmit Mode, this field defines whether T8 and T16 are in the Ping-Pong mode or in independent normal operation mode. Setting this field to “Normal Operation Mode” terminates the “Ping-Pong Mode” operation. When set to 10, T16 is immediately forced to a 0; a setting of 11 forces T16 to output a 1.

In Demodulation Mode, this field defines the width of the glitch that must be filtered out.

Initial_T8_Out/Rising_Edge

In Transmit Mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When the counter is not enabled and this bit is set to 1 or 0, T8_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D1.

In Demodulation Mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset the mode, a 1 should be written to this location.

Initial_T16 Out/Falling_Edge

In Transmit Mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or Ping-Pong Mode (CTR1, D3; D2). When the counter is not enabled and this bit is set, T16_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D0.

In Demodulation Mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

► **Note:** Modifying CTR1 (D1 or D0) while the counters are enabled causes unpredictable output from T8/16_OUT.

CTR2 Counter/Timer 16 Control Register—CTR2(0D)02h

Table 12 lists and briefly describes the fields for this register.



Table 12. CTR2(0D)02h: Counter/Timer16 Control Register

Field	Bit Position		Value	Description
T16_Enable	7-----	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6-----	R/W	0	Transmit Mode
			1	Modulo-N
			0	Single Pass
			1	Demodulation Mode
Time_Out	--5-----	R	0**	T16 Recognizes Edge
			1	T16 Does Not Recognize Edge
		W	0	No Counter Timeout
			1	Counter Timeout Occurred
T16_Clock	---43---	R/W	00**	No Effect
			01	Reset Flag to 0
			10	SCLK
			11	SCLK/2
Capture_INT_Mask	-----2--	R/W	0**	SCLK/4
			1	SCLK/8
Counter_INT_Mask	-----1-	R/W	0*	Disable Data Capture Int.
			1	Enable Data Capture Int.
P35_Out	-----0	R/W	0*	Disable Timeout Int.
			1	Enable Timeout Int.

Note:

*Indicates the value upon Power-On Reset.

** Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

T16_Enable

This field enables T16 when set to 1.

Single/Modulo-N

In Transmit Mode, when set to 0, the counter reloads the initial value when it reaches the terminal count. When set to 1, the counter stops when the terminal count is reached.



In Demodulation Mode, when set to 0, T16 captures and reloads on detection of all the edges. When set to 1, T16 captures and detects on the first edge but ignores the subsequent edges. For details, see the description of T16 Demodulation Mode on page 40.

Time_Out

This bit is set when T16 times out (terminal count reached). To reset the bit, write a 1 to this location.

T16_Clock

This bit defines the frequency of the input signal to Counter/Timer16.

Capture_INT_Mask

This bit is set to allow an interrupt when data is captured into LO16 and HI16.

Counter_INT_Mask

Set this bit to allow an interrupt when T16 times out.

P35_Out

This bit defines whether P35 is used as a normal output pin or T16 output.

CTR3 T8/T16 Control Register—CTR3(0D)03h

Table 13 lists and briefly describes the fields for this register. This register allows the T8 and T16 counters to be synchronized.

Table 13. CTR3(0D)03h T8/T16 Control Register

T16_Enable	7-----	R	0*	Counter Disabled
		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
T8 Enable	-6-----	R/W	0**	Counter Disabled
			1	Counter Enabled
			0	Stop Counter
			1	Enable Counter
Sync Mode	--5-----	R/W	0*	Disable Sync Mode
			1	Enable Sync Mode
Reserved	---43210	R/W	1	Always reads 11111
			x	No Effect

* Indicates the value upon Power-On Reset.

*** Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

Counter/Timer Functional Blocks

Input Circuit

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5–D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal that have a width less than specified (CTR1 D3, D2) are filtered out (see Figure 15).

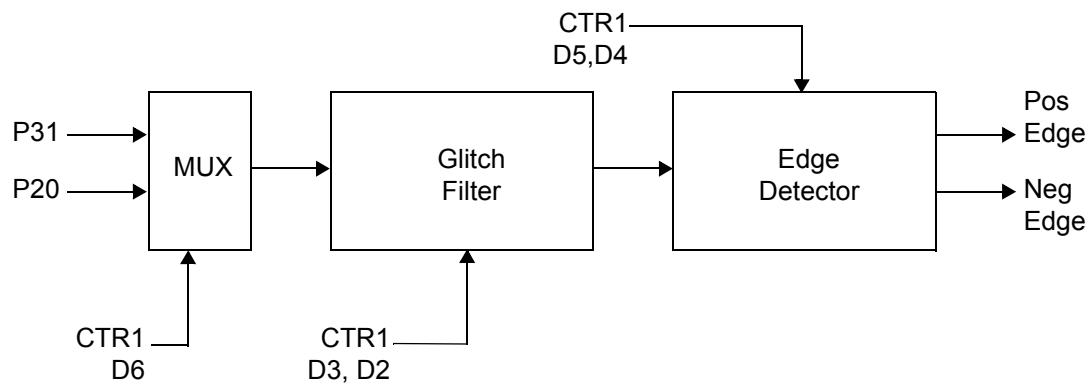


Figure 15. Glitch Filter Circuitry

T8 Transmit Mode

Before T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8_OUT is 1; if it is 1, T8_OUT is 0. See Figure 16.

When T8 is enabled, the output T8_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In Single-Pass Mode (CTR0, D6), T8 counts down to 0 and stops, T8_OUT toggles, the timeout status bit (CTR0, D5) is set, and a timeout interrupt can be generated if it is enabled (CTR0, D1). In Modulo-N Mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, and sets the timeout status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is complete. T8 then loads from TC8H or TC8L according to the T8_OUT level and repeats the cycle. See Figure 17.

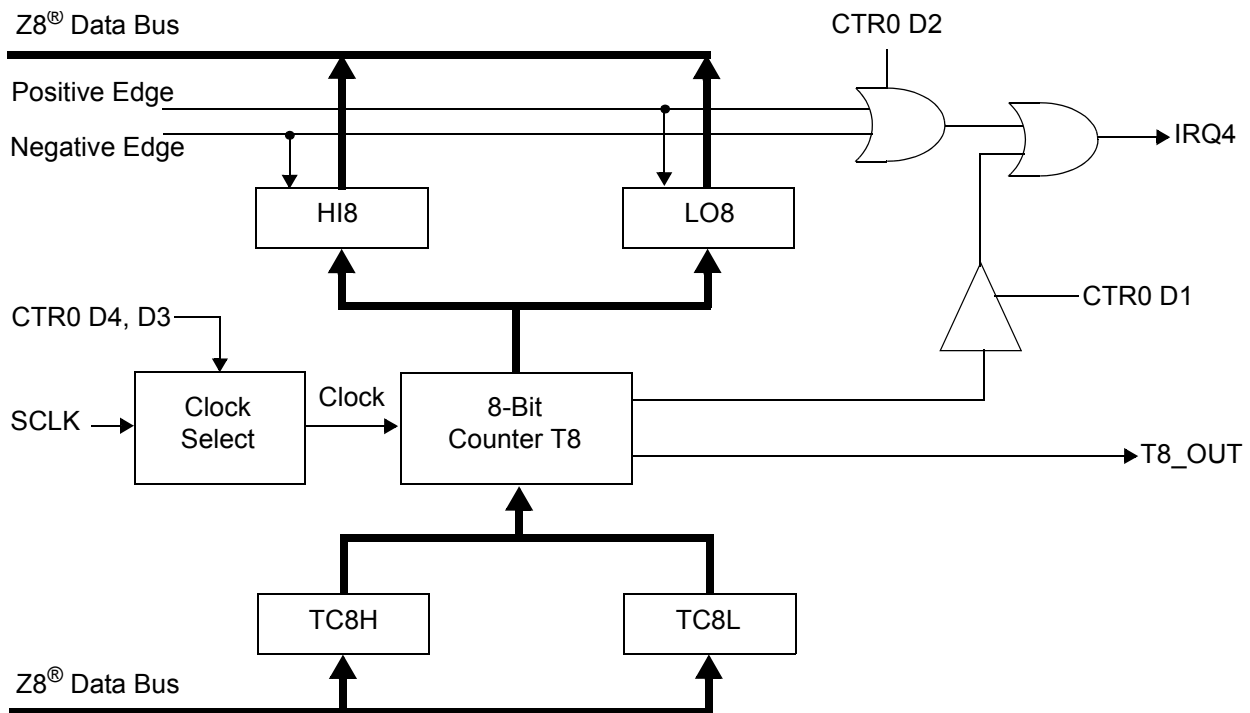


Figure 17. 8-Bit Counter/Timer Circuits

The values in TC8H or TC8L can be modified at any time. The new values take effect when they are loaded.



Caution: To ensure known operation do not write these registers at the time the values are to be loaded into the counter/timer. *An initial count of 1 is not allowed (a non-function occurs).* An initial count of 0 causes TC8 to count from 0 to FFh to FEh.

► **Note:** The letter *h* denotes hexadecimal values.

Transition from 0 to FF_h is not a timeout condition.



Caution: Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur. See Figure 18 and Figure 19.

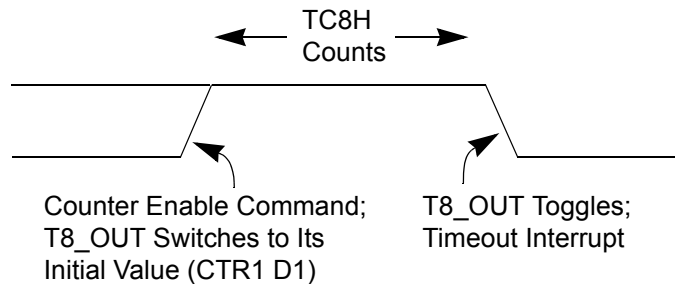


Figure 18. T8_OUT in Single-Pass Mode

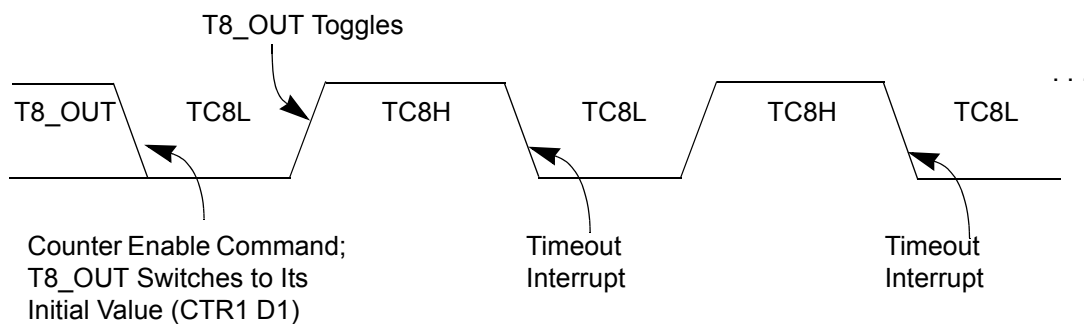


Figure 19. T8_OUT in Modulo-N Mode

T8 Demodulation Mode

The user must program TC8L and TC8H to FF_h. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put into LO8; if it is a negative edge, data is put into HI8. From that point, one of the

edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the timeout status bit (CTR0, D5) is set, and an interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from FFh (see Figure 21 and Figure 21).

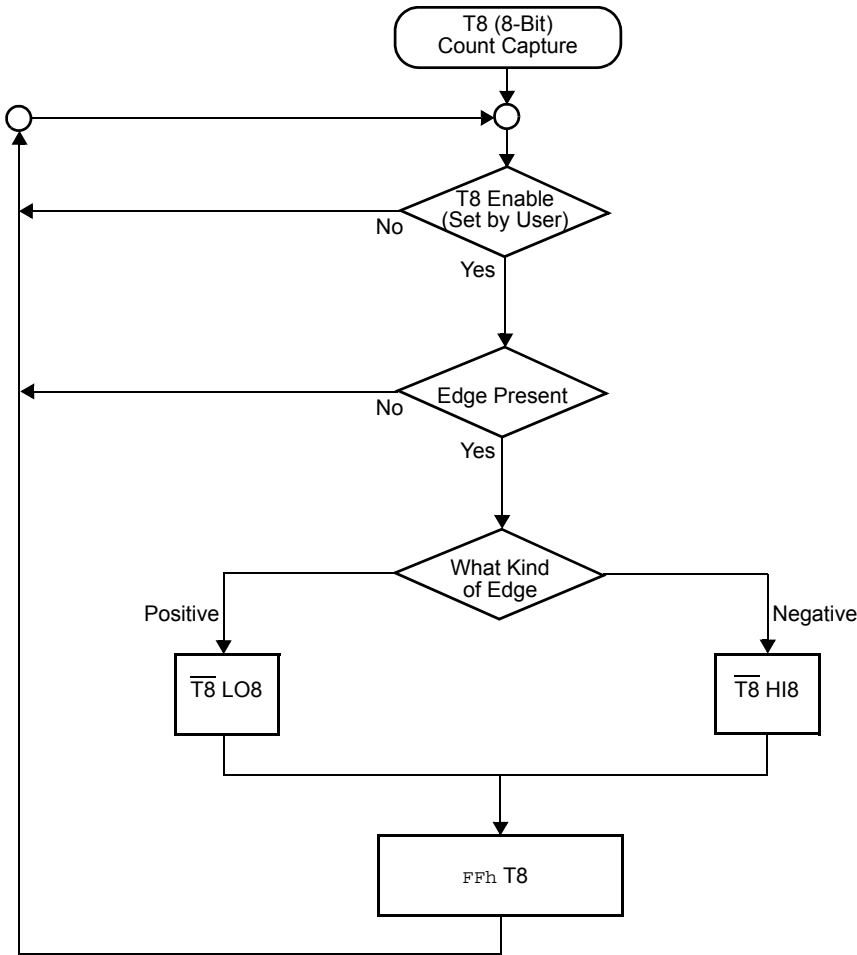


Figure 20. Demodulation Mode Count Capture Flowchart

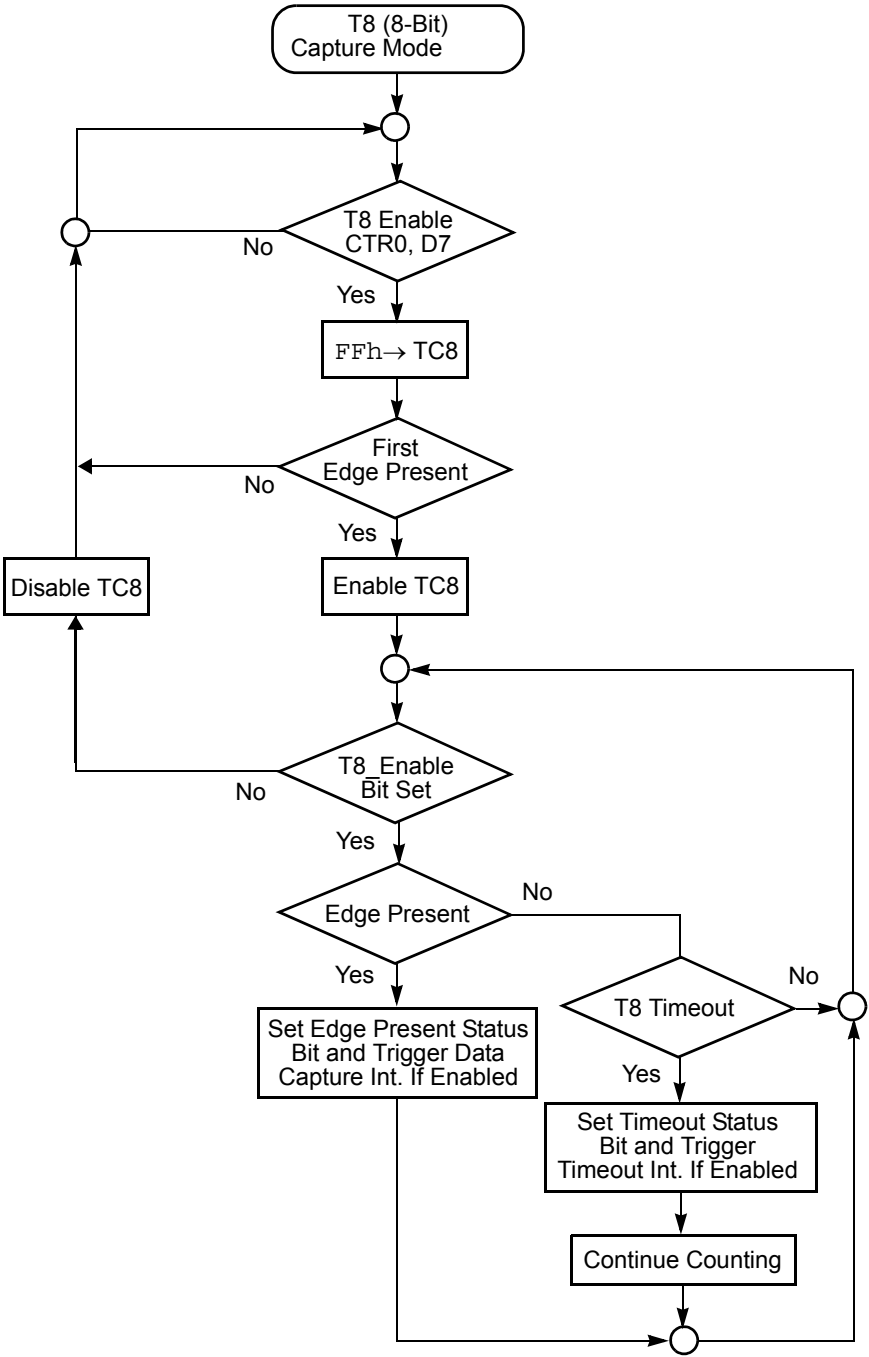


Figure 21. Demodulation Mode Flowchart

T16 Transmit Mode

In Normal or Ping-Pong mode, the output of T16 when not enabled, is dependent on CTR1, D0. If it is a 0, T16_OUT is a 1; if it is a 1, T16_OUT is 0. You can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3; D2 to a 10 or 11.

When T16 is enabled, TC16H * 256 + TC16L is loaded, and T16_OUT is switched to its initial value (CTR1, D0). When T16 counts down to 0, T16_OUT is toggled (in NORMAL or PING-PONG mode), an interrupt (CTR2, D1) is generated (if enabled), and a status bit (CTR2, D5) is set. See Figure 22.

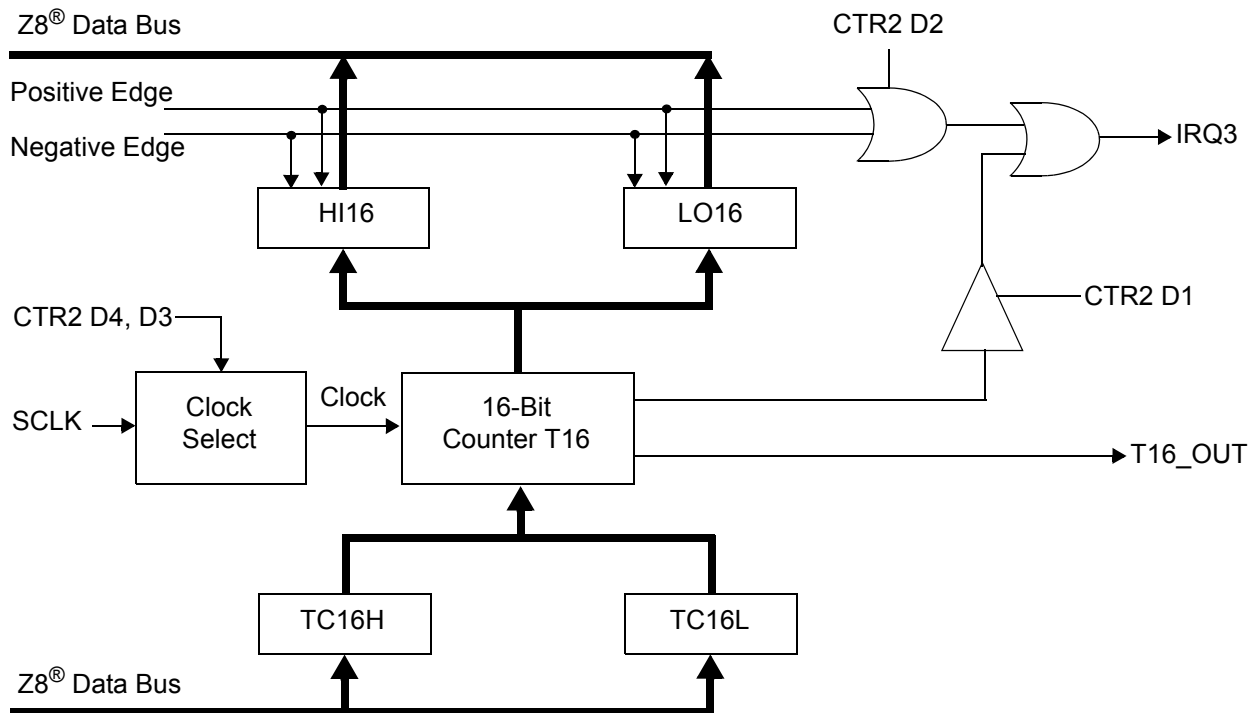


Figure 22. 16-Bit Counter/Timer Circuits

► **Note:** Global interrupts override this function as described in “Interrupts” on page 43.

If T16 is in Single-Pass mode, it is stopped at this point (see Figure 23). If it is in Modulo-N Mode, it is loaded with TC16H * 256 + TC16L, and the counting continues (see Figure 24).

The values in TC16H and TC16L can be modified at any time. The new values take effect when they are loaded.



Caution:

Do not load these registers at the time the values are to be loaded into the counter/timer to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to `FFFFh` to `FFFEh`. Transition from 0 to `FFFFh` is not a timeout condition.

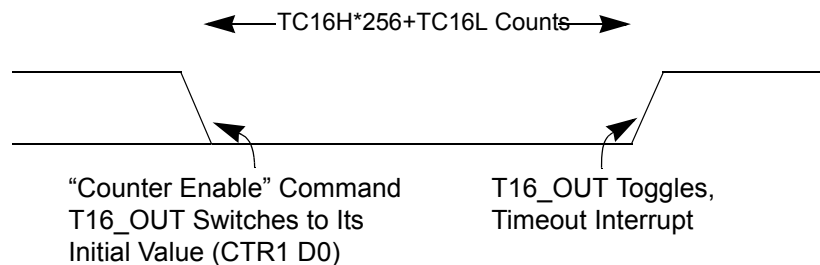


Figure 23. T16_OUT in Single-Pass Mode

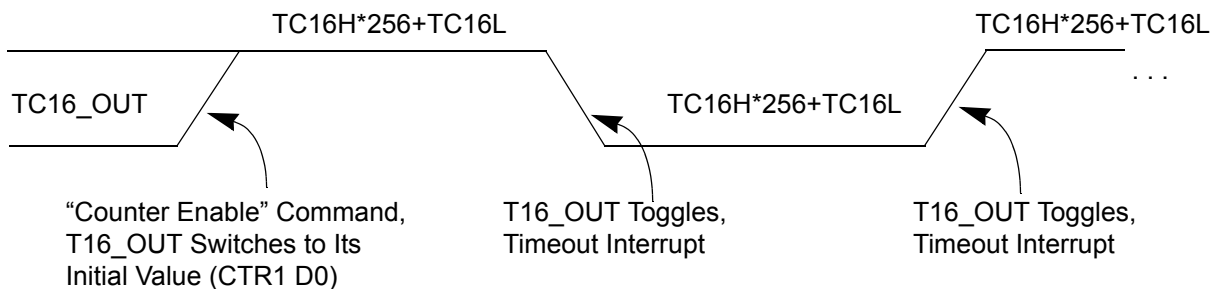


Figure 24. T16_OUT in Modulo-N Mode

T16 Demodulation Mode

The user must program TC16L and TC16H to `FFh`. After T16 is enabled, and the first edge (rising, falling, or both depending on CTR1 D5; D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

If D6 of CTR2 Is 0

When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current count in T16 is complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt is generated if enabled (CTR2, D2). T16 is loaded with `FFFFh` and starts again.

This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).



If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A timeout of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both depending on CTR1, D5; D4), continuing to ignore subsequent edges.

This T16 mode generally measures mark time, the length of an active carrier signal burst.

If T16 reaches 0, T16 continues counting from `FFFFh`. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt timeout can be generated if enabled (CTR2 D1).

Ping-Pong Mode

This operation mode is only valid in Transmit Mode. T8 and T16 must be programmed in Single-Pass mode (CTR0, D6; CTR2, D6), and Ping-Pong mode must be programmed in CTR1, D3; D2. The user can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR2, D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1, D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the ping-pong operation, write 00 to bits D3 and D2 of CTR1. See Figure 25.

- **Note:** Enabling ping-pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and reset the status flags before instituting this operation.

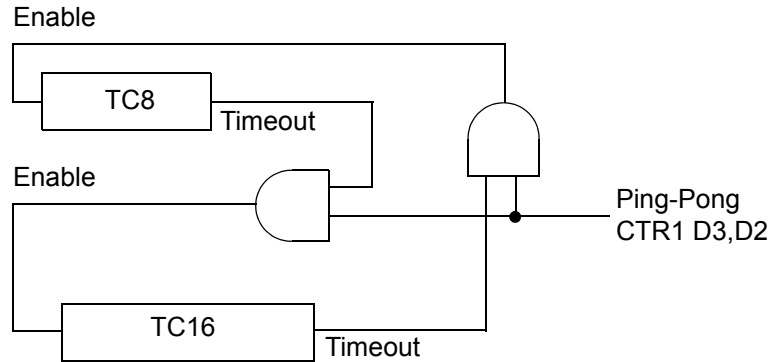


Figure 25. Ping-Pong Mode Diagram

Initiating Ping-Pong Mode

First, make sure both counter/timers are not running. Set T8 into Single-Pass mode (CTR0, D6), set T16 into Single-Pass mode (CTR2, D6), and set the Ping-Pong mode (CTR1, D2; D3). These instructions can be in random order. Finally, start Ping-Pong mode by enabling either T8 (CTR0, D7) or T16 (CTR2, D7). See Figure 25.

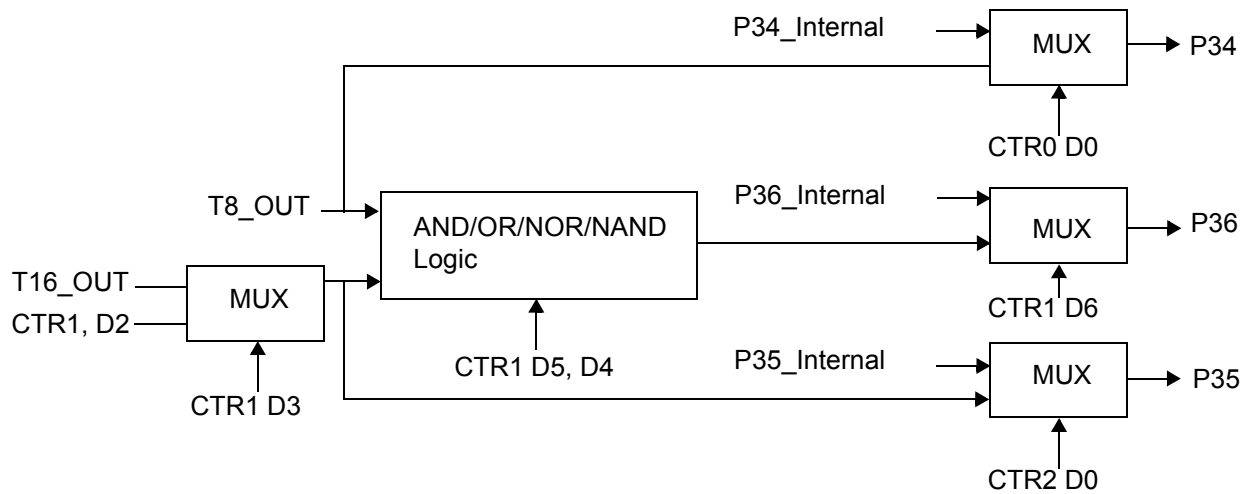


Figure 26. Output Circuit

The initial value of T8 or T16 must not be 1. If you stop the timer and restart the timer, reload the initial value to avoid an unknown previous value.



During Ping-Pong Mode

The enable bits of T8 and T16 (CTR0, D7; CTR2, D7) are set and cleared alternately by hardware. The timeout bits (CTR0, D5; CTR2, D5) are set every time the counter/timers reach the terminal count.

Timer Output

The output logic for the timers is illustrated in Figure 26. P34 is used to output T8-OUT when D0 of CTR0 is set. P35 is used to output the value of T16-OUT when D0 of CTR2 is set. When D6 of CTR1 is set, P36 outputs the logic combination of T8-OUT and T16-OUT determined by D5 and D4 of CTR1.

Interrupts

The Crimzon™ ZLR16300 features six different interrupts (Table 14). The interrupts are maskable and prioritized (Figure 27). The six sources are divided as follows: three sources are claimed by Port 3 lines P33–P31, two by the counter/timers (Table 14) and one for low voltage detection. The Interrupt Mask Register (globally or individually) enables or disables the six interrupt requests.

The source for IRQ is determined by bit 1 of the Port 3 mode register (P3M). When in digital mode, Pin P33 is the source. When in analog mode the output of the Stop Mode Recovery source logic is used as the source for the interrupt. See Figure 32, Stop Mode Recovery Source, on page 52.

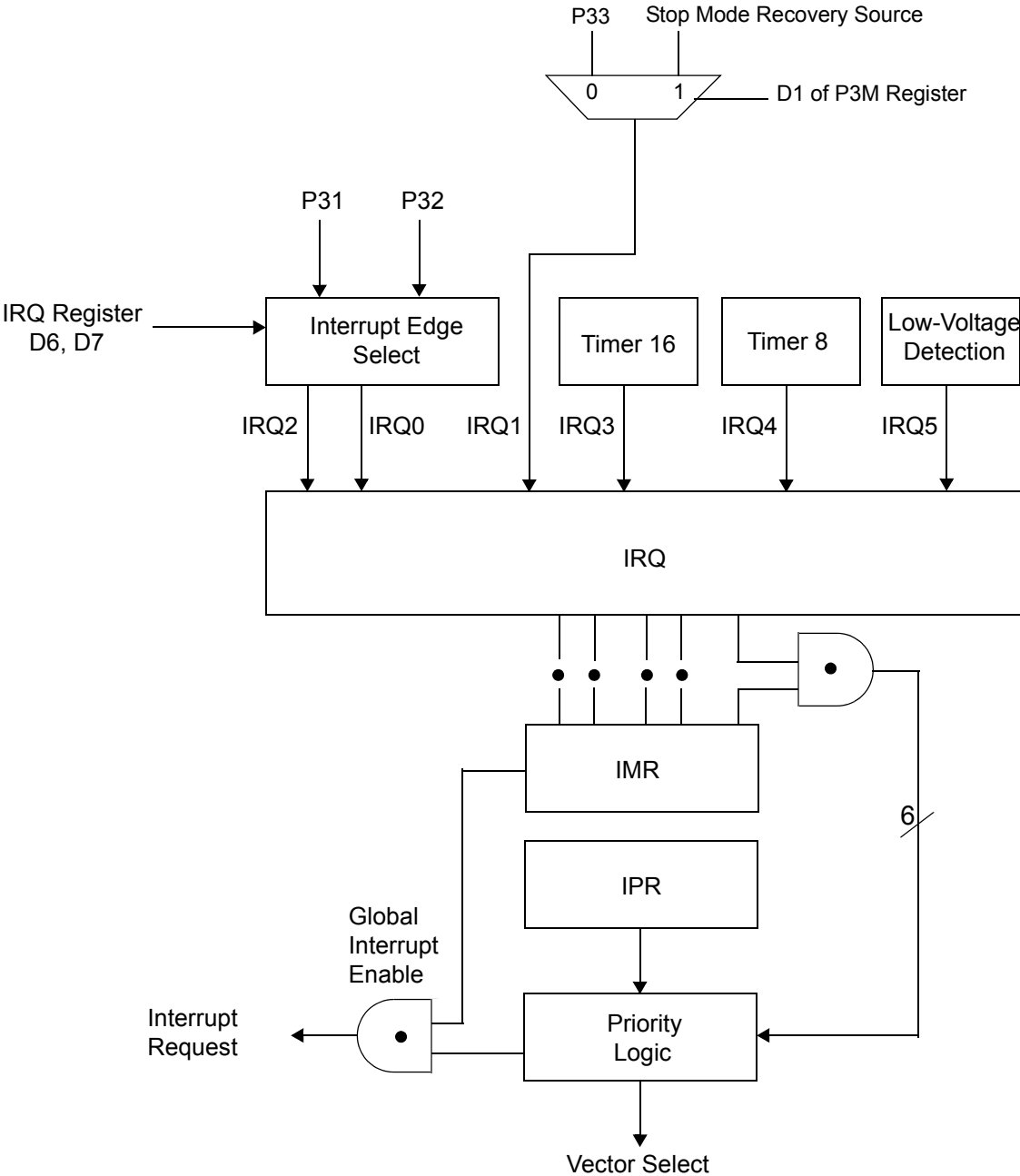


Figure 27. Interrupt Block Diagram

**Table 14. Interrupt Types, Sources, and Vectors**

Name	Source	Vector Location	Comments
IRQ0	P32	0,1	External (P32), Rising, Falling Edge Triggered
IRQ1	P33	2,3	External (P33), Falling Edge Triggered
IRQ2	P31, T _{IN}	4,5	External (P31), Rising, Falling Edge Triggered
IRQ3	T16	6,7	Internal
IRQ4	T8	8,9	Internal
IRQ5	LVD	10,11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority Register. An interrupt machine cycle activates when an interrupt request is granted. As a result, all subsequent interrupts are disabled, and the Program Counter and Status Flags are saved. The cycle then branches to the program memory vector location reserved for that interrupt. All Crimzon™ ZLR16300 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked, and the Interrupt Request register is polled to determine which of the interrupt requests require service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 can be rising, falling, or both edge triggered. These interrupts are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is indicated in Table 15.

Table 15. IRQ Register

IRQ		Interrupt Edge	
D7	D6	IRQ2 (P31)	IRQ0 (P32)
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Note: F = Falling Edge; R = Rising Edge

Clock

The device's on-chip oscillator has a high-gain, parallel-resonant amplifier, for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal must be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100 Ω . The on-chip oscillator can be driven with a suitable external clock source.

The crystal must be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance greater than or equal to 22 pF) from each pin to ground.

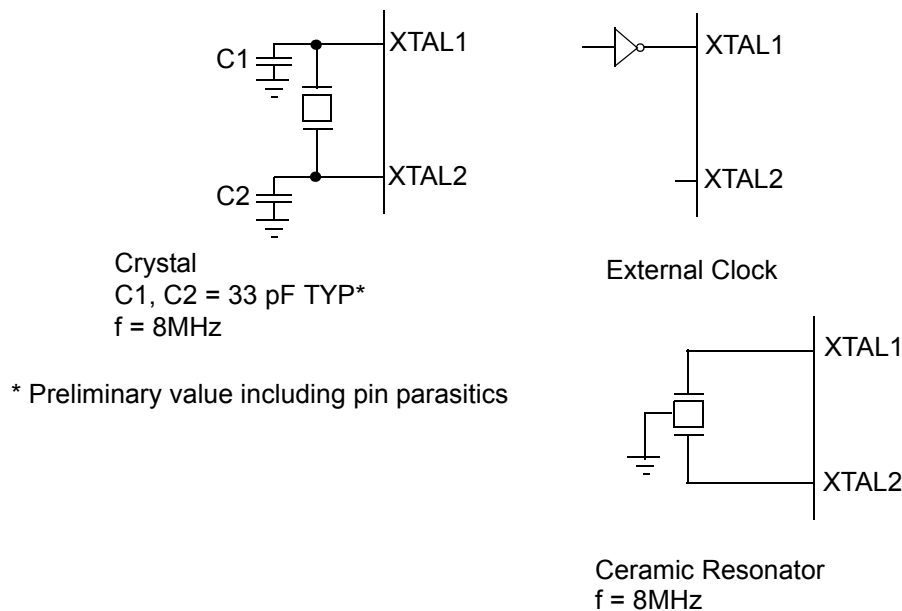


Figure 28. Oscillator Configuration

Power-On Reset

A timer circuit clocked by a dedicated on-board RC-oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{DD} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK status, including Waking up from V_{BO} Standby
- Stop-Mode Recovery (if D5 of SMR = 1)
- WDT Timeout



The POR timer is 2.5 ms minimum. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock).

Halt Mode

This instruction turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, IRQ4, and IRQ5 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit Halt Mode. After the interrupt service routine, the program continues from the instruction after the Halt.

Stop Mode

This instruction turns off the internal clock and external crystal oscillation, reducing the standby current to 10 μ A or less. Stop Mode is terminated only by a reset, such as WDT timeout, POR or SMR. This condition causes the processor to restart the application program at address 000Ch. In order to enter Stop (or Halt) mode, first flush the instruction pipeline to avoid suspending execution in mid-instruction. Execute an NOP instruction (Opcode = FFh) immediately before the appropriate sleep instruction, as follows:



```
FF      NOP      ; clear the pipeline
6F      STOP     ; enter Stop Mode
```

or

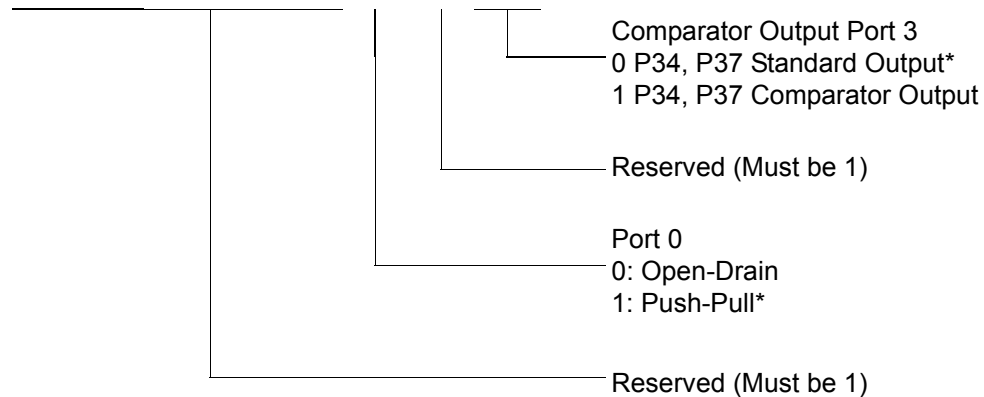
```
FF      NOP      ; clear the pipeline
7F      HALT     ; enter Halt Mode
```

Port Configuration Register

The Port Configuration (PCON) register (Figure 29) configures the comparator output on Port 3. It is located in the expanded register file at Bank F, location 00.

PCON (0F) 00H

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



* Default setting after reset

Figure 29. Port Configuration Register (PCON) (Write Only)

Comparator Output Port 3 (D0)

Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration.

Port 0 Output Mode (D2)

Bit 2 controls the output mode of port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

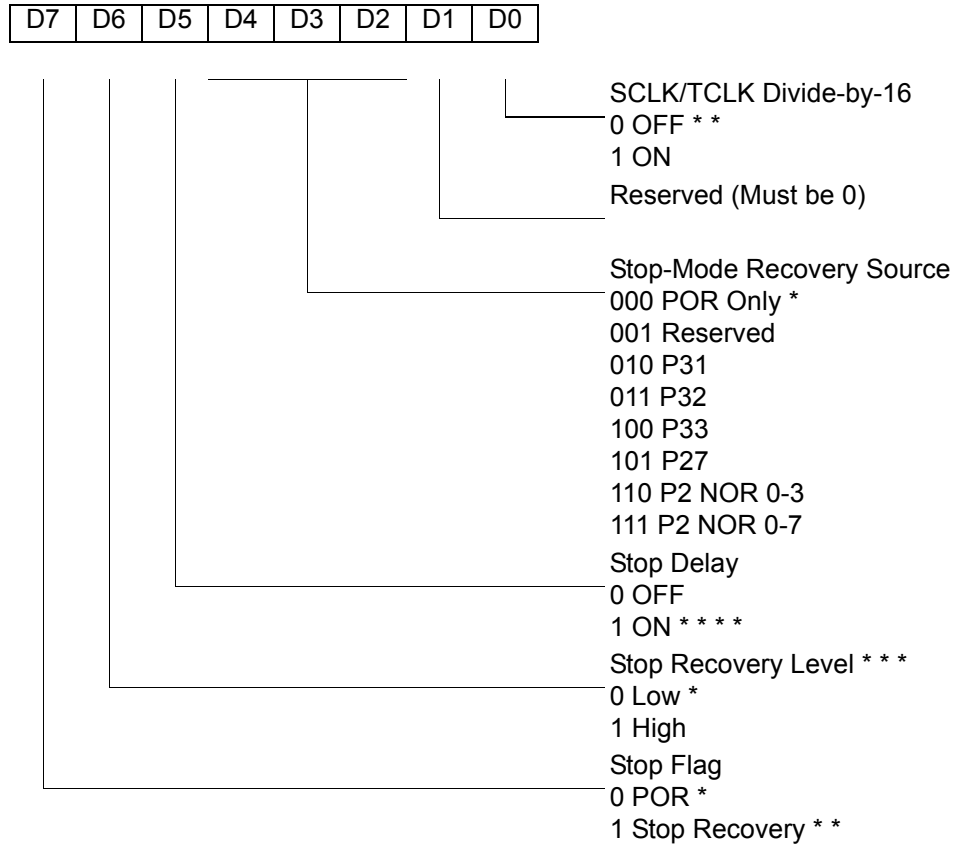


Stop-Mode Recovery Register (SMR)

This register selects the clock divide value and determines the mode of Stop Mode Recovery (Figure 30). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of Stop recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level at the XOR-gate input (Figure 32 on page 52) is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop-Mode Recovery signal. Bits D0 determines if SCLK/TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register File at address 0Bh.



SMR (0F) 0BH



* Default after Power On Reset or Watch-Dog Reset

* * Default setting after Reset and Stop Mode Recovery

* * * At the XOR gate input

* * * * Default setting after reset. Must be 1 if using a crystal or resonator clock source.

Figure 30. Stop Mode Recovery Register

SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK (Figure 31). This control selectively reduces device power consumption during normal processor execution (SCLK control) and/or Halt Mode (where TCLK sources interrupt logic). After Stop-Mode Recovery, this bit is set to 0.

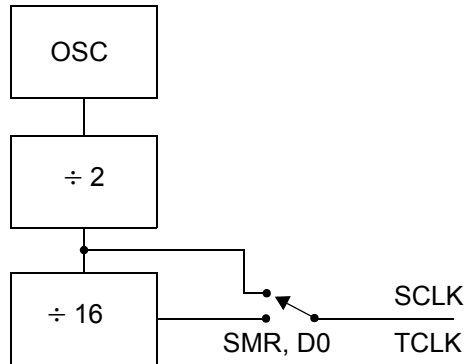


Figure 31. SCLK Circuit

Stop-Mode Recovery Register 2—SMR2(0F)0DH

Table 16 lists and describes the fields for this register.

Table 16. SMR2(F)0DH:Stop Mode Recovery Register 2*

Field	Bit Position	Value	Description
Reserved	7-----	0	Reserved (Must be 0)
Recovery Level	-6-----	W 0 [†] 1	Low High
Reserved	--5-----	0	Reserved (Must be 0)
Source	---432--	W 000 [†] 001 010 011 100 101 110 111	A. POR Only B. NAND of P23–P20 C. NAND of P27–P20 D. NOR of P33–P31 E. NAND of P33–P31 F. NOR of P33–P31, P00, P07 G. NAND of P33–P31, P00, P07 H. NAND of P33–P31, P22–P20
Reserved	-----10	00	Reserved (Must be 0)

Notes:

* Port pins configured as outputs are ignored as an SMR recovery source.

[†] Indicates the value at Power-On Reset

Stop-Mode Recovery Source (D2, D3, and D4)

These three bits of the SMR specify the wake-up source of the Stop recovery (Figure 32 and Table 17).

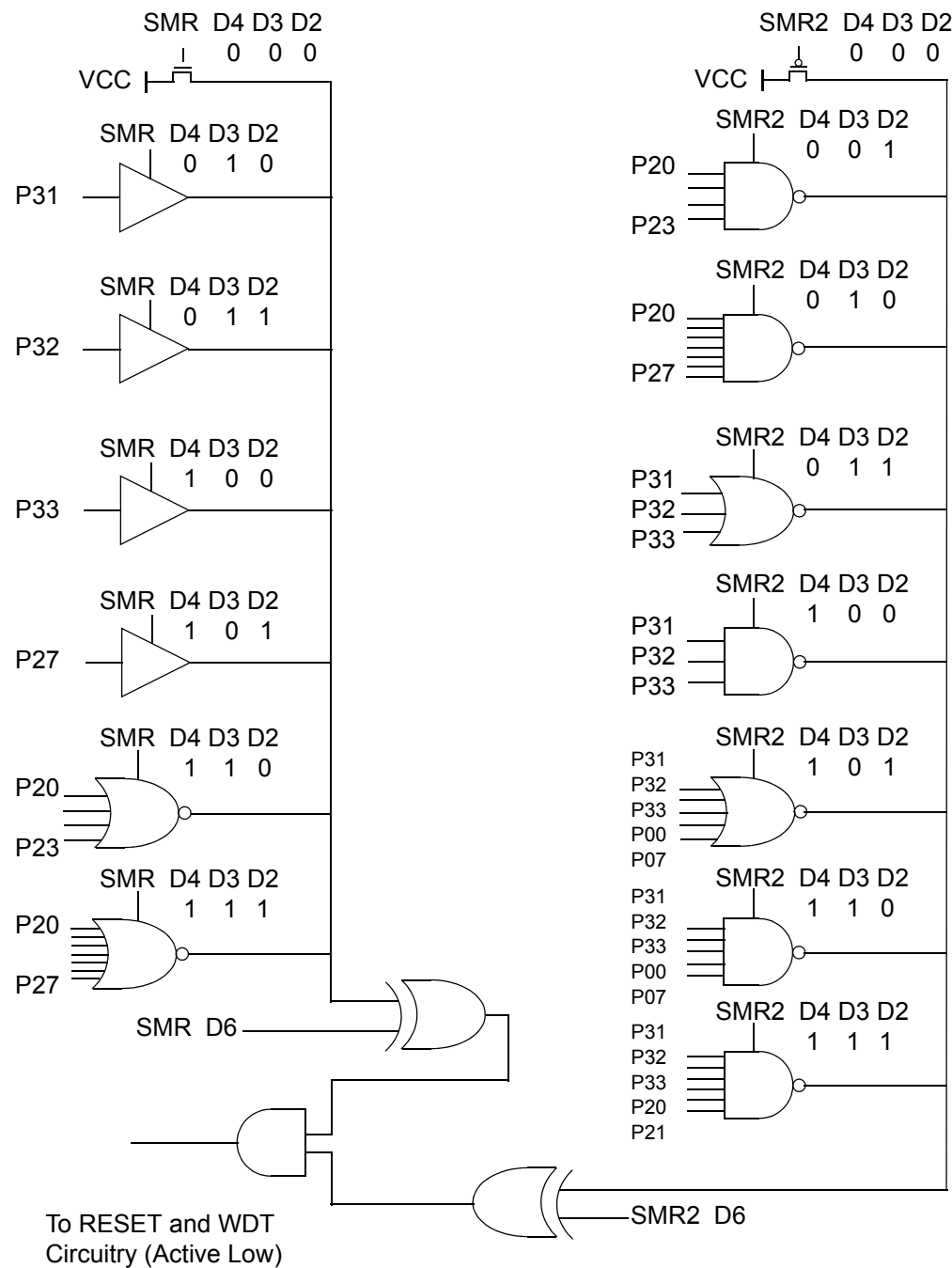


Figure 32. Stop Mode Recovery Source



Table 17. Stop Mode Recovery Source

SMR:432			Operation
D4	D3	D2	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	Reserved
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

- **Note:** Any Port 2 bit defined as an output drives the corresponding input to the default state. This condition allows the remaining inputs to control the AND/OR function. Refer to SMR2 register on page 54 for other recover sources.

Stop Mode Recovery Delay Select (D5)

This bit, if Low, disables the T_{POR} delay after Stop Mode Recovery. The default configuration of this bit is 1. If the “fast” wake up is selected, the Stop Mode Recovery source must be kept active for at least 10 T_{pC} .

- **Note:** This bit must be set to 1 if using a crystal or resonator clock source. The T_{POR} delay allows the clock source to stabilize before executing instructions.

Stop Mode Recovery Edge Select (D6)

A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the Crimzon™ ZLR16300 from Stop Mode. A 0 indicates Low level recovery. The default is 0 on POR.

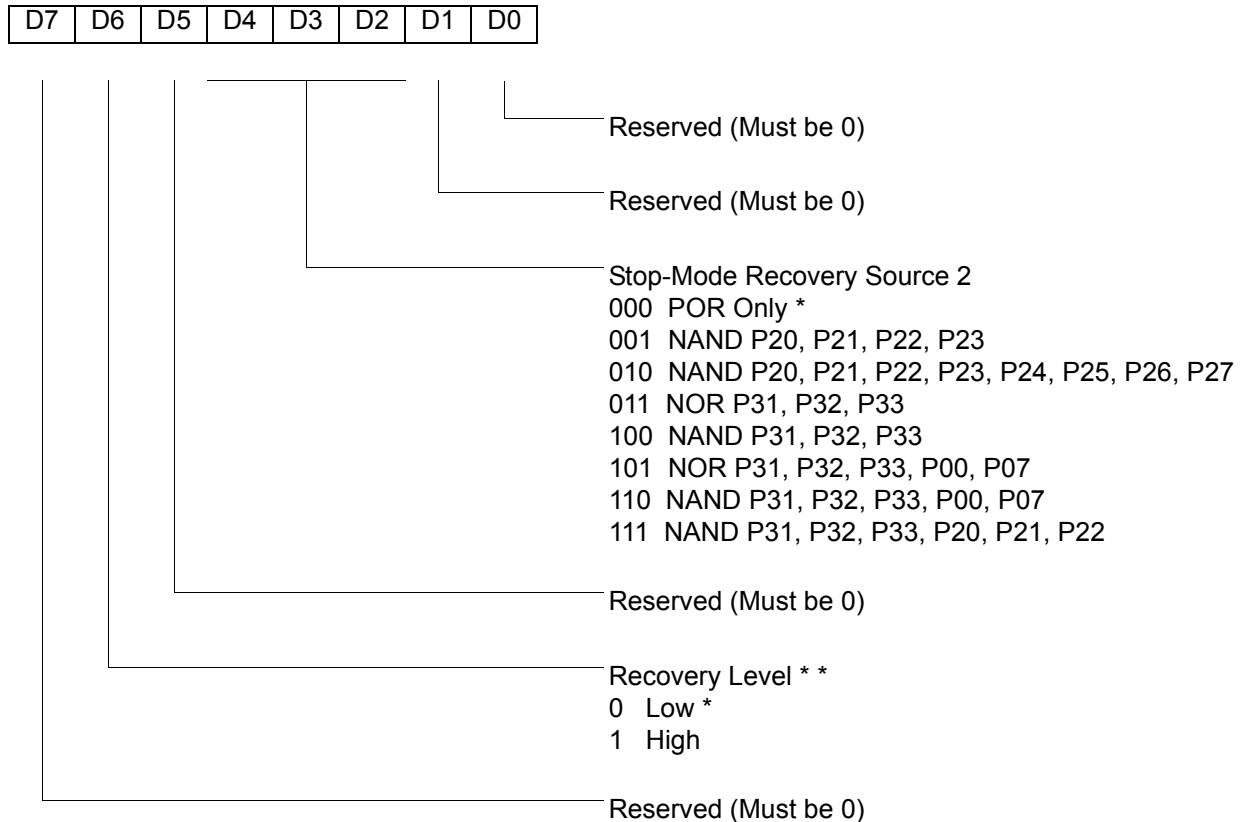
Cold or Warm Start (D7)

This bit is read only. It is set to 1 when the device is recovered from Stop Mode. The bit is set to 0 when the device reset is other than Stop Mode Recovery (SMR).

Stop Mode Recovery Register 2 (SMR2)

This register determines the mode of Stop Mode Recovery for SMR2 (Figure 33).

SMR2 (0F) DH



Note: If used in conjunction with SMR, either of the two specified events causes a Stop-Mode Recovery.

* Default setting after reset

* * At the XOR gate input

Figure 33. Stop Mode Recovery Register 2 ((0F) DH:D2–D4, D6 Write Only)

If SMR2 is used in conjunction with SMR, either of the specified events causes a Stop Mode Recovery.

- **Note:** Port pins configured as outputs are ignored as an SMR or SMR2 recovery source. For example, if the NAND or P23–P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23–P21) form the NAND equation.

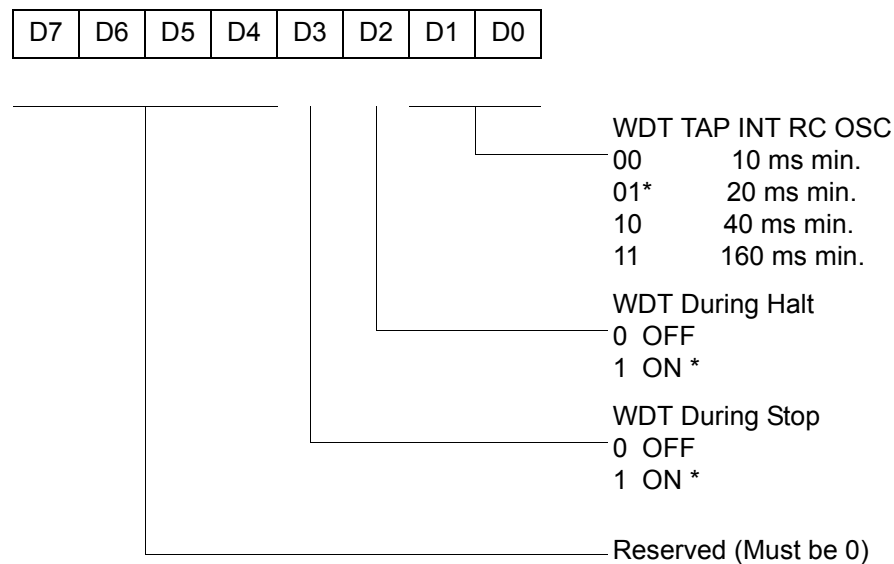


Watch-Dog Timer Mode Register (WDTMR)

The Watch-Dog Timer (WDT) is a retriggerable one-shot timer that resets the Z8® if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction. On subsequent executions of the WDT instruction, the WDT is refreshed. The WDT circuit is driven by an on-board RC-oscillator. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source the internal RC-oscillator. Bits 0 and 1 of the WDT register control a tap circuit that determines the minimum timeout period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during STOP. Bits 4 through 7 are reserved (Figure 34). This register is accessible only during the first 60 processor cycles (120 XTAL clocks) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset, or a Stop-Mode Recovery (Figure 33). After this point, the register cannot be modified by any means (intentional or otherwise). The WDTMR cannot be read. The register is located in Bank F of the Expanded Register File at address location 0Fh. It is organized as illustrated in Figure 34.

WDTMR (0F) 0FH



* Default setting after reset

Figure 34. Watch-Dog Timer Mode Register (Write Only)

WDT Time Select (D0, D1)

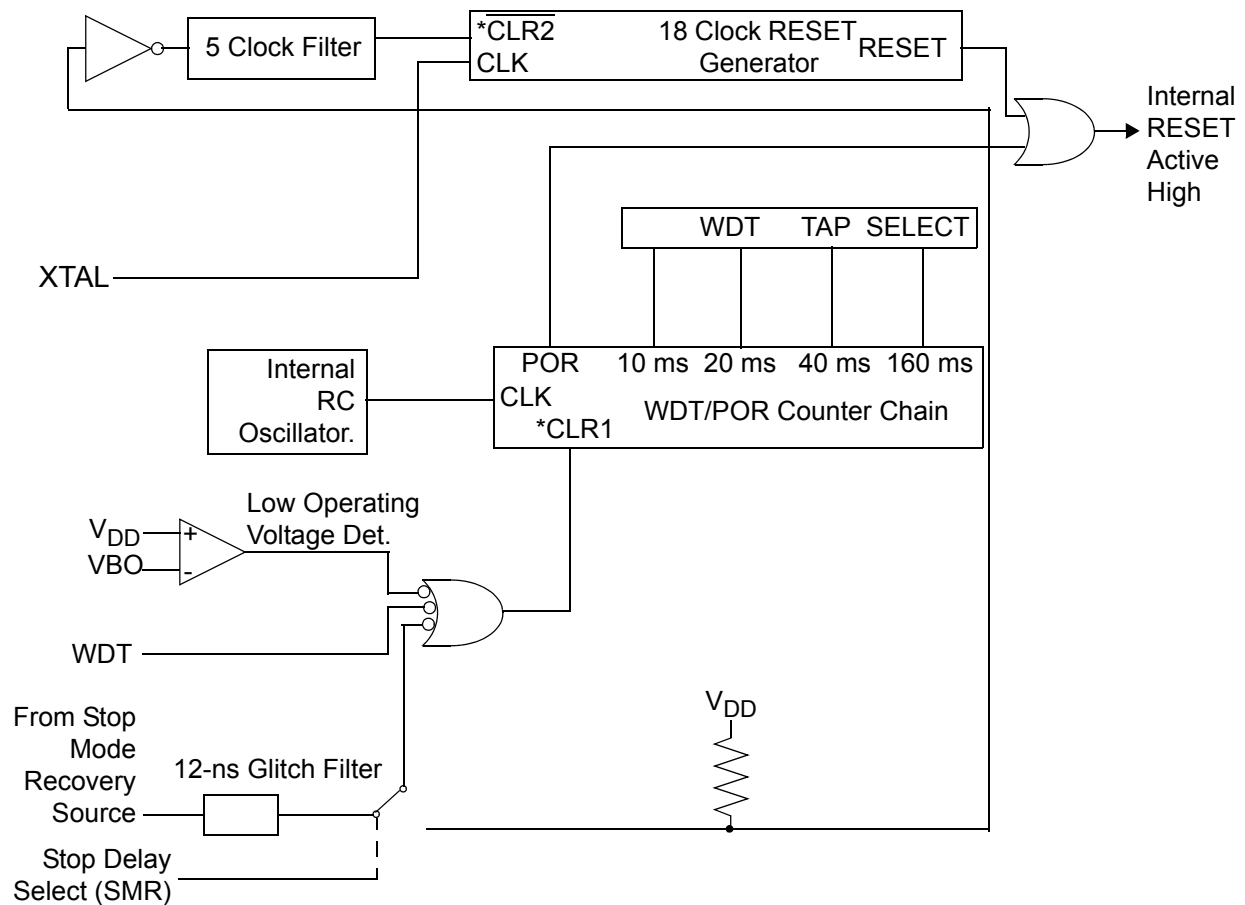
This bit selects the WDT time period. It is configured as indicated in Table 18.

Table 18. Watch-Dog Timer Time Select

D1	D0	Timeout of Internal RC-Oscillator
0	0	10 ms min.
0	1	20 ms min.
1	0	40 ms min.
1	1	160 ms min.

WDTMR During Halt (D2)

This bit determines whether or not the WDT is active during Halt Mode. A 1 indicates active during Halt. The default is 1. See Figure 35.



* CLR1 and $\overline{\text{CLR2}}$ enable the WDT/POR and 18 Clock Reset timers respectively upon a Low-to-High input translation.

Figure 35. Resets and WDT



WDTMR During Stop (D3)

This bit determines whether or not the WDT is active during Stop Mode. A 1 indicates active during Stop. The default is 1.

ROM Selectable Options

There are five ROM Selectable Options to choose from based on ROM code requirements. These options are listed in Table 19.

Table 19. ROM Selectable Options

Port 00–03 Pull-Ups	On/Off
Port 04–07 Pull-Ups	On/Off
Port 20–27 Pull-Up Port 3 Pull-Ups	On/Off
Port 3 Pull-Ups	On/Off
Watch-Dog Timer at Power-On Reset	On/Off

Voltage Brown-Out/Standby

An on-chip Voltage Comparator checks that the V_{DD} is at the required level for correct operation of the device. Reset is globally driven when V_{DD} falls below V_{BO} . A small drop in V_{DD} causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the V_{DD} is allowed to stay above V_{RAM} , the RAM content is preserved. When the power level is returned to above V_{BO} , the device performs a POR and functions normally.

Low-Voltage Detection Register—LVD(0D)0CH

► **Note:** Voltage detection does not work at Stop mode. It must be disabled during Stop mode in order to reduce current.

Field	Bit Position			Description
LVD	765432---			Reserved
	-----2	R	1 0*	HVD flag set HVD flag reset
	-----1-	R	1 0*	LVD flag set LVD flag reset
	-----0	R/W	1 0*	Enable VD Disable VD

*Default after POR



- **Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

Voltage Detection and Flags

The Voltage Detection register (LVD, register 0Ch at the expanded register bank 0Dh) offers an option of monitoring the V_{CC} voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. When Voltage Detection is enabled, the V_{CC} level is monitored in real time. The flags in the LVD register valid 20uS after Voltage Detection is enabled. The HVD flag (bit 2 of the LVD register) is set only if V_{CC} is lower than the V_{HVD} . When Voltage Detection is enabled, the LVD flag also triggers IRQ5. The IRQ bit 5 latches the low voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a flag only.

- **Note:** If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt instruction (EI) prior to enabling the voltage detection.

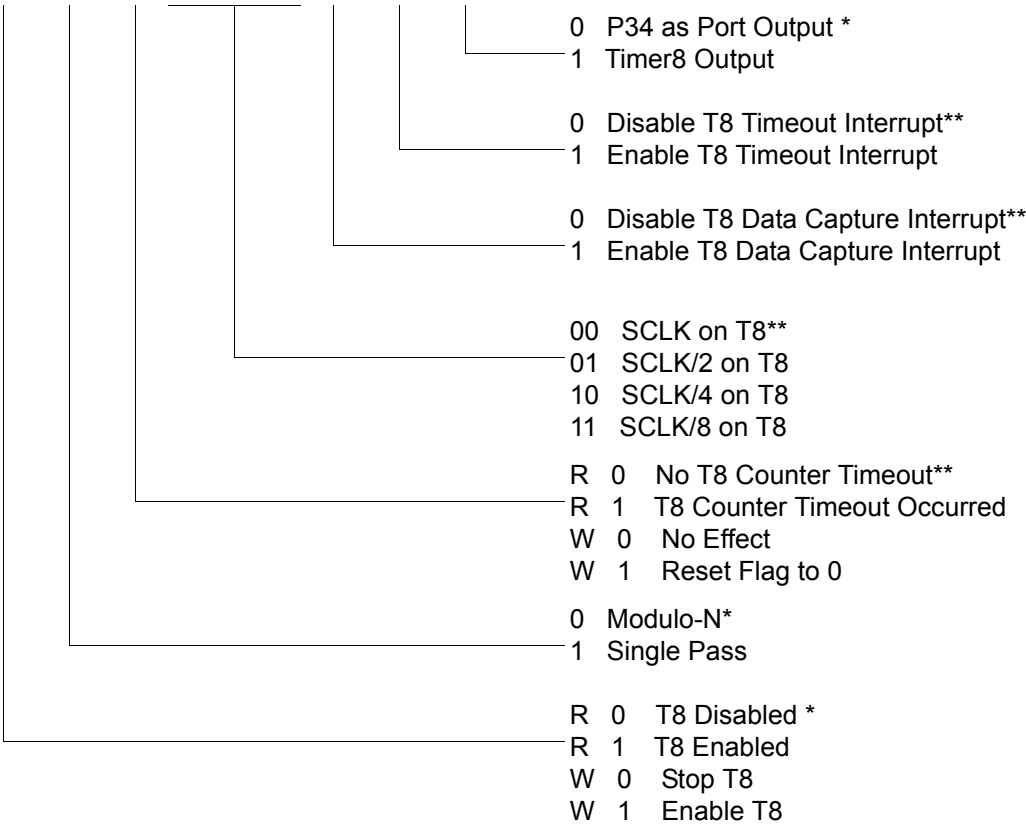
Expanded Register File Control Registers (0D)

The expanded register file control registers (0D) are depicted in Figure 36 through Figure 40.



CTR0 (0D) 00H

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



* Default setting after reset.

** Default setting after Reset. Not reset with a Stop Mode recovery

Figure 36. TC8 Control Register ((0D) 00H: Read/Write Except Where Noted)



CTR1 (0D) 01H

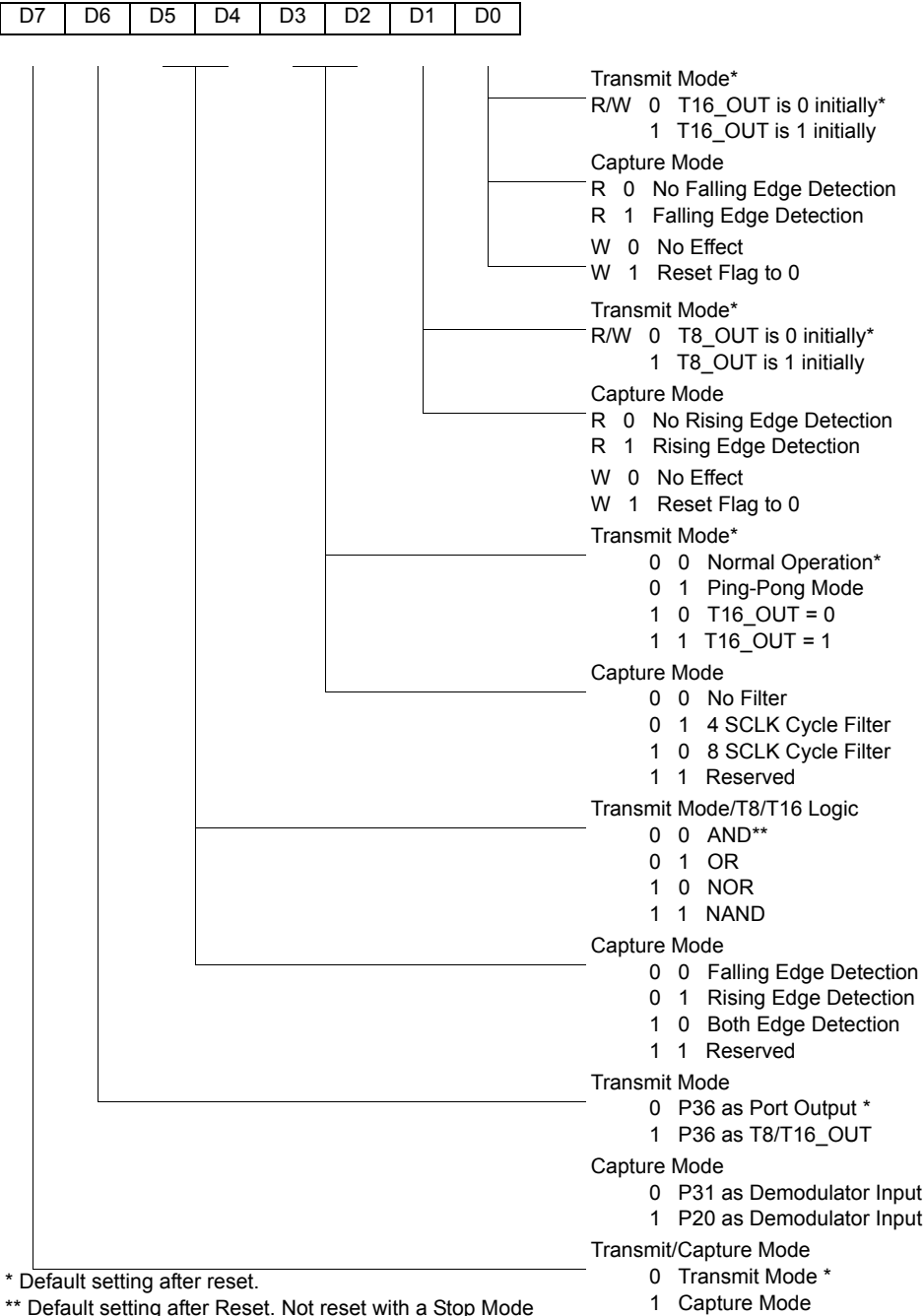


Figure 37. T8 and T16 Common Control Functions ((0D) 01H: Read/Write)

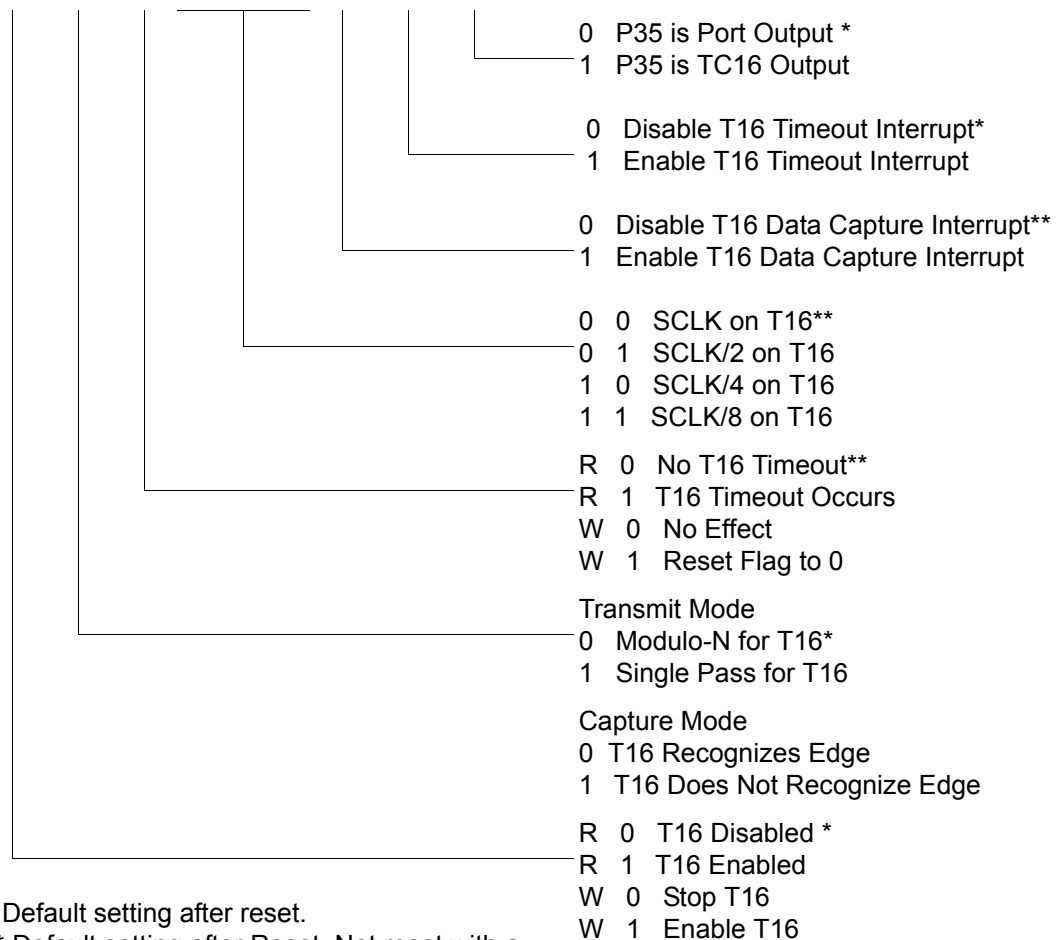


- **Notes:** Take care in differentiating the Transmit Mode from Capture Mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.

Changing from one mode to another cannot be performed without disabling the counter/timers.

CTR2 (0D) 02H

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



* Default setting after reset.

** Default setting after Reset. Not reset with a Stop Mode recovery.

Figure 38. T16 Control Register ((0D) 02H: Read/Write Except Where Noted)



CTR3 (0D) 03H

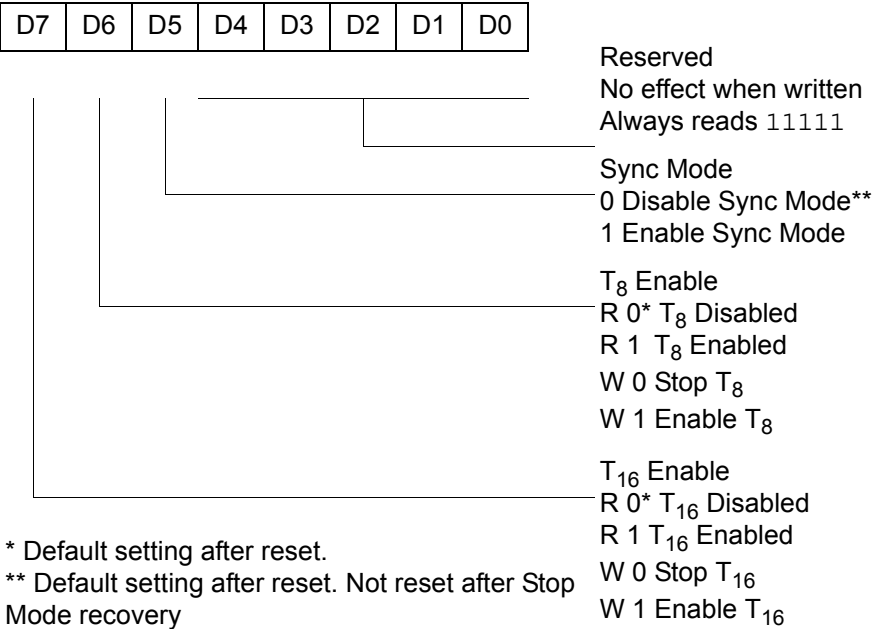


Figure 39. T8/T16 control Register (0D) 03H: Read/Write (Except Where Noted)

► **Note:** If Sync Mode is enabled, the first pulse of T8 (carrier) is always synchronized with T16 (demodulated signal). It can always provide a full carrier pulse.

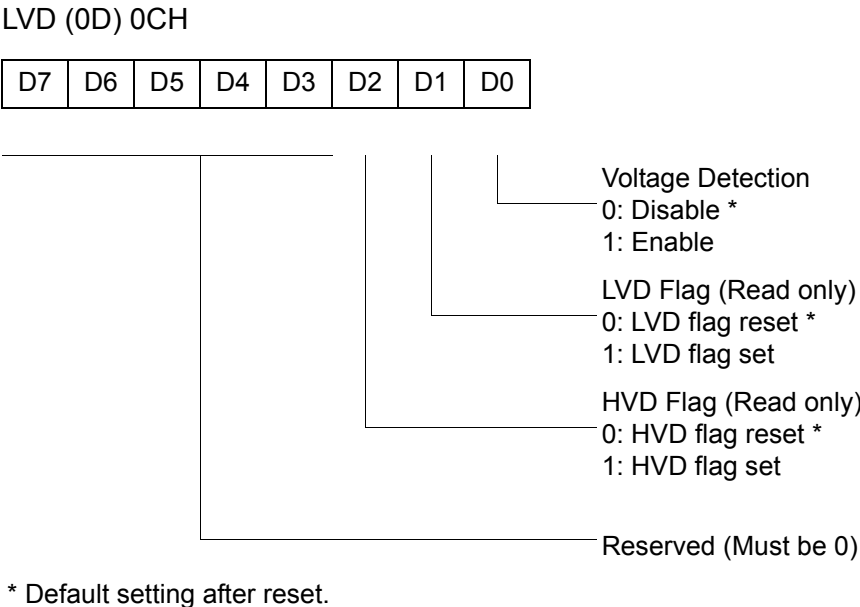
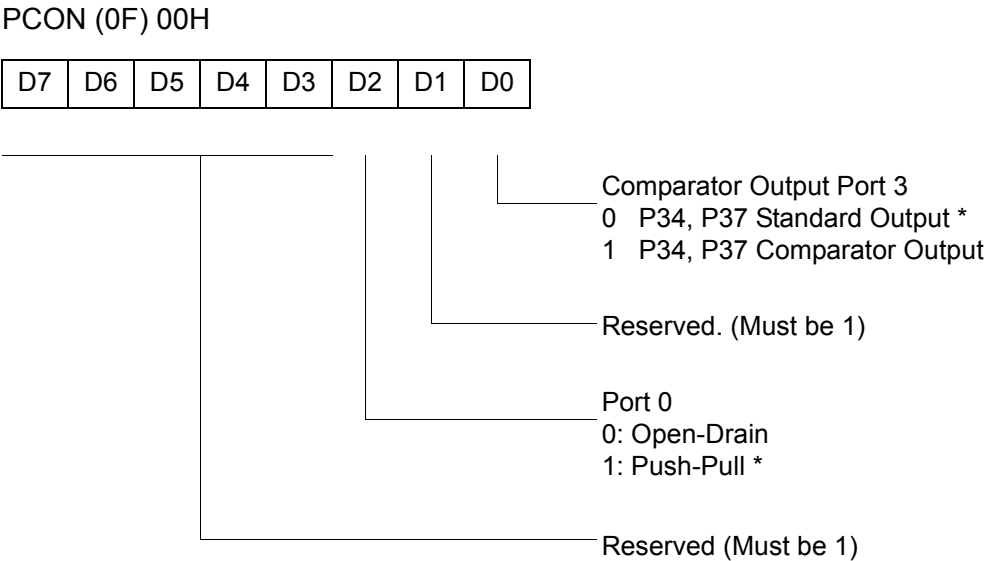


Figure 40. Voltage Detection Register

Expanded Register File Control Registers (0F)

The expanded register file control registers (0F) are depicted in Figures 41 through Figure 54.

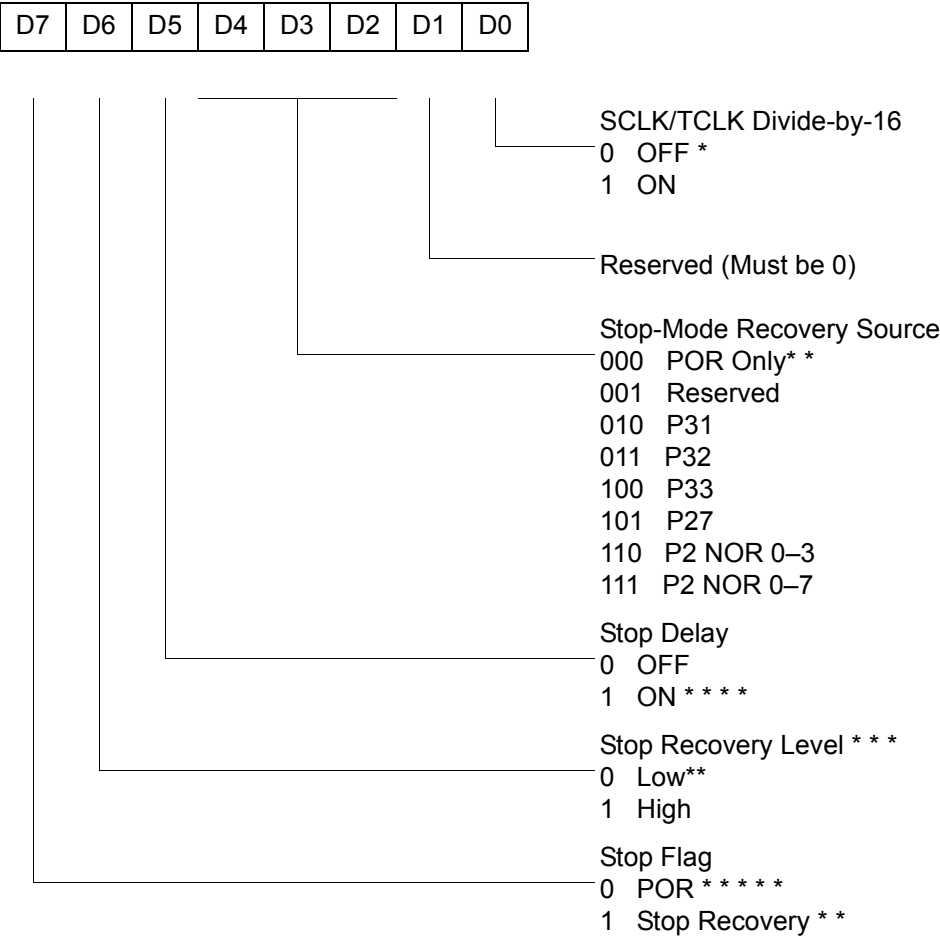


* Default setting after reset

Figure 41. Port Configuration Register (PCON) ((0F)00H: Write Only

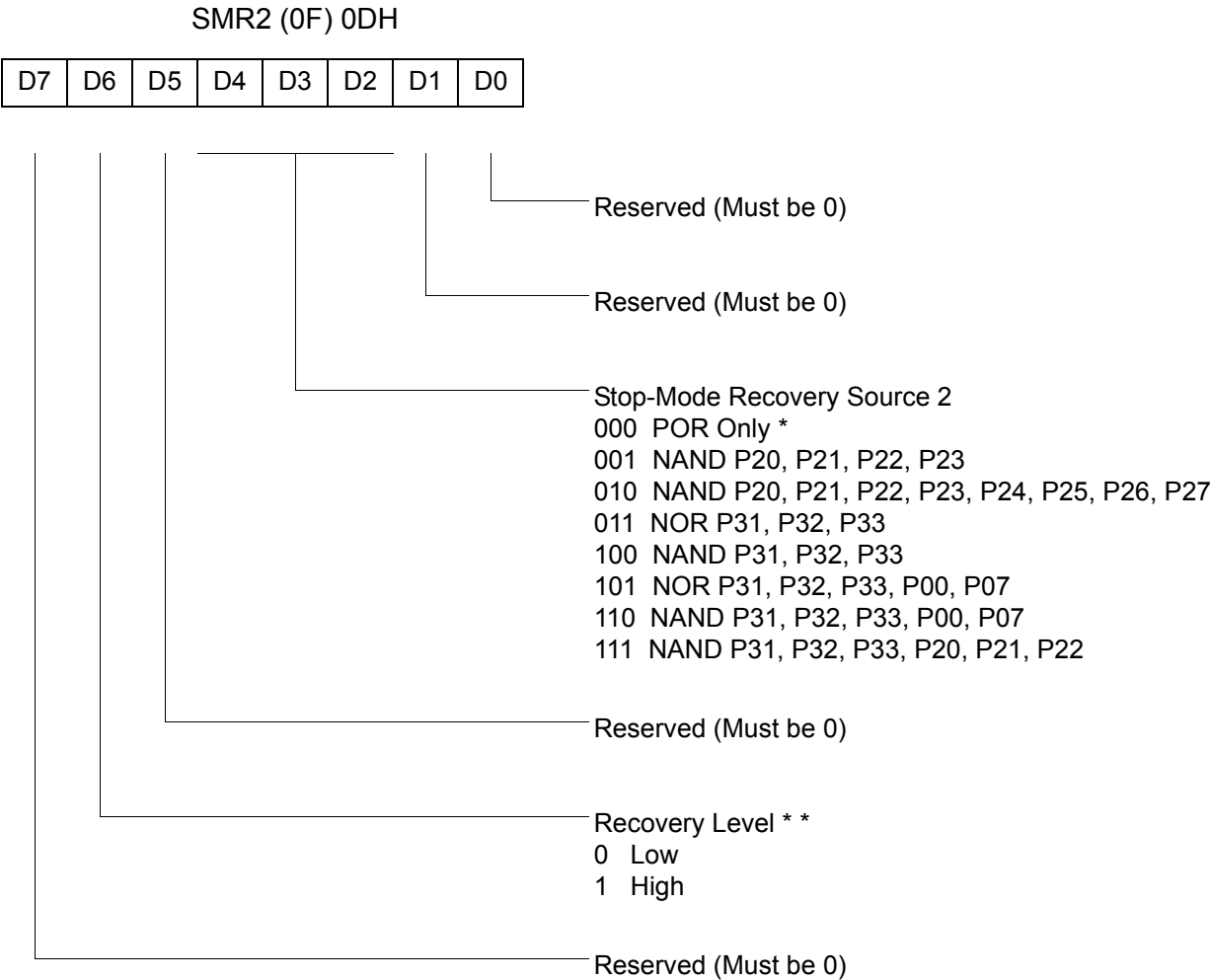


SMR (0F) 0BH



* Default setting after Reset
* * Set after STOP Mode Recovery
* * * At the XOR gate input
* * * * Default setting after reset. Must be 1 if using a crystal or resonator clock source.
Not reset with a Stop Mode recovery.
* * * * * Default setting after Power On Reset

Figure 42. Stop Mode Recovery Register ((0F) 0BH: D6–D0=Write Only, D7=Read Only)

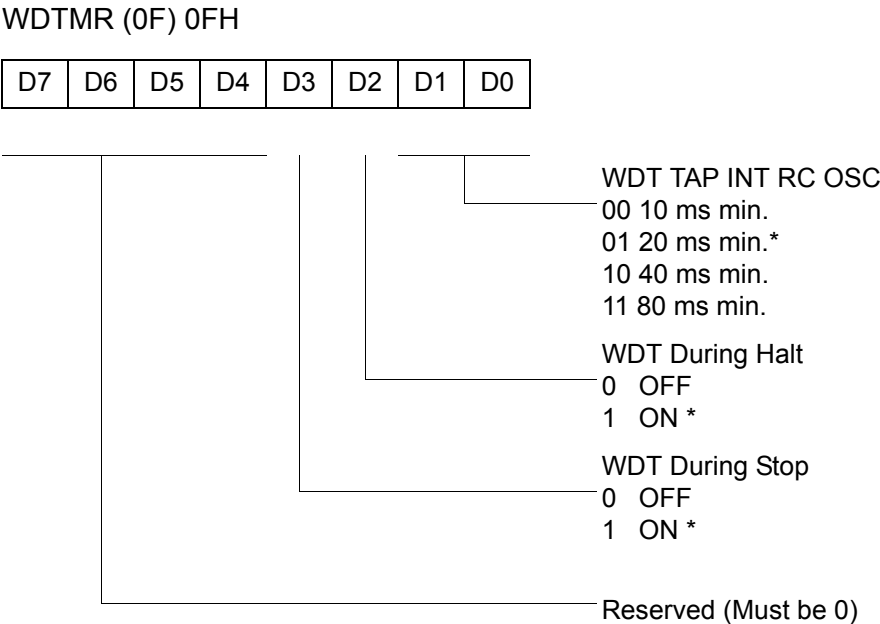


Note: If used in conjunction with SMR, either of the two specified events causes a Stop-Mode Recovery.

* Default setting after reset. Not reset with a Stop Mode recovery.

* * At the XOR gate input

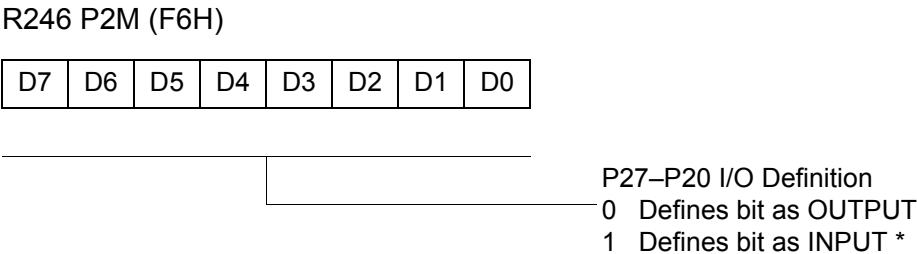
Figure 43. Stop Mode Recovery Register 2 ((0F) 0DH: D2–D4, D6 Write Only)



* Default setting after reset. Not reset with a Stop Mode recovery.

Figure 44. Watch-Dog Timer Register ((0F) 0FH: Write Only)

Standard Control Registers



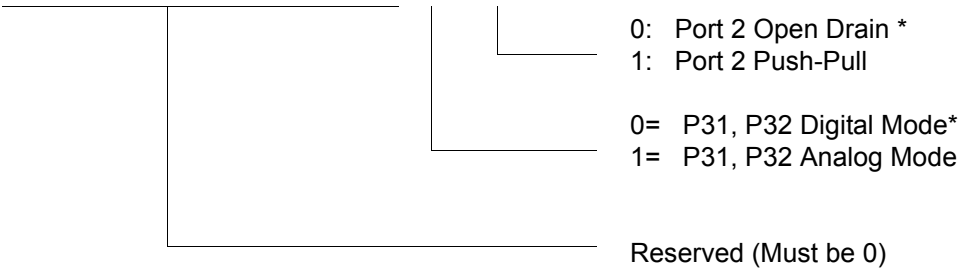
* Default setting after reset. Not reset with a Stop Mode recovery.

Figure 45. Port 2 Mode Register (F6H: Write Only)



R247 P3M (F7H)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

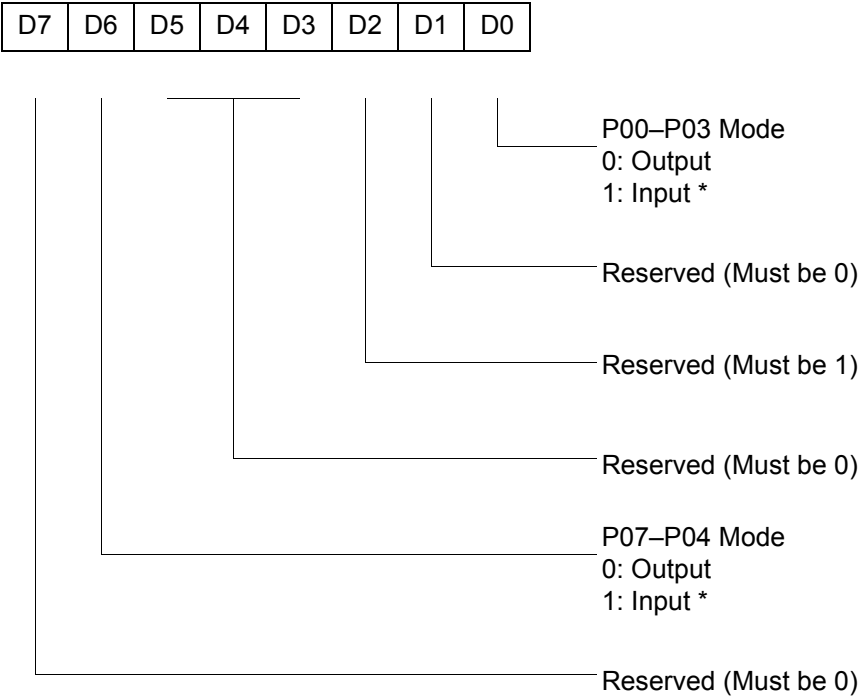


* Default setting after reset. Not reset with a Stop Mode recovery.

Figure 46. Port 3 Mode Register (F7H: Write Only)



R248 P01M (F8H)



* Default setting after reset; only P00, P01 and P07 are available on 20-pin configurations.

Figure 47. Port 0 Register (F8H: Write Only)



R249 IPR (F9H)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

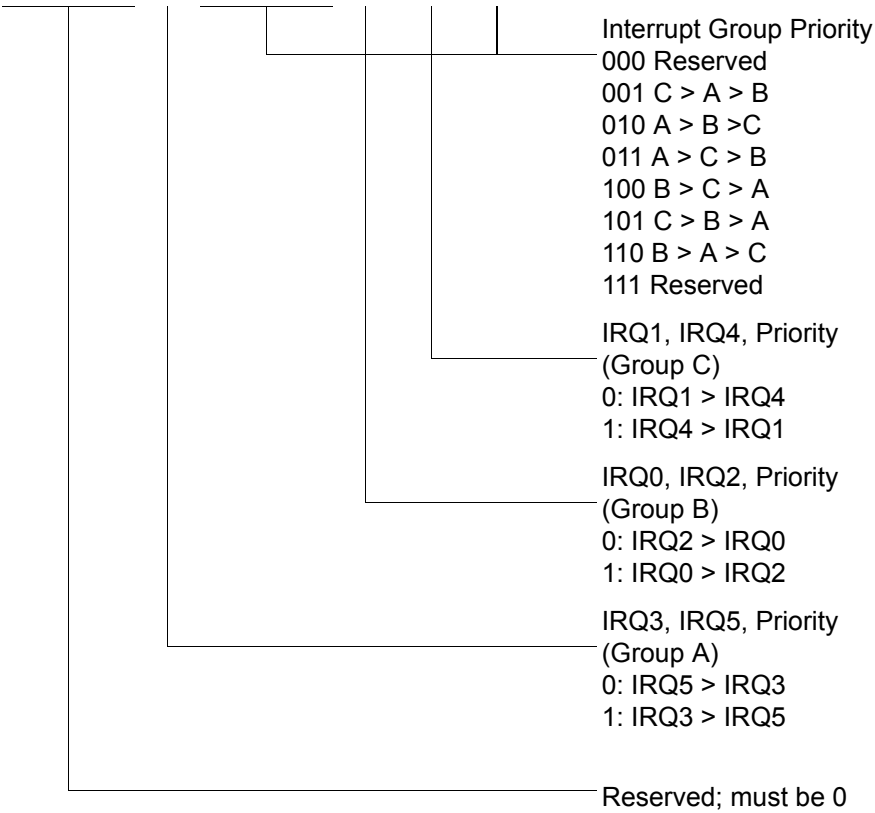


Figure 48. Interrupt Priority Register (F9H: Write Only)



R250 IRQ (FAH)

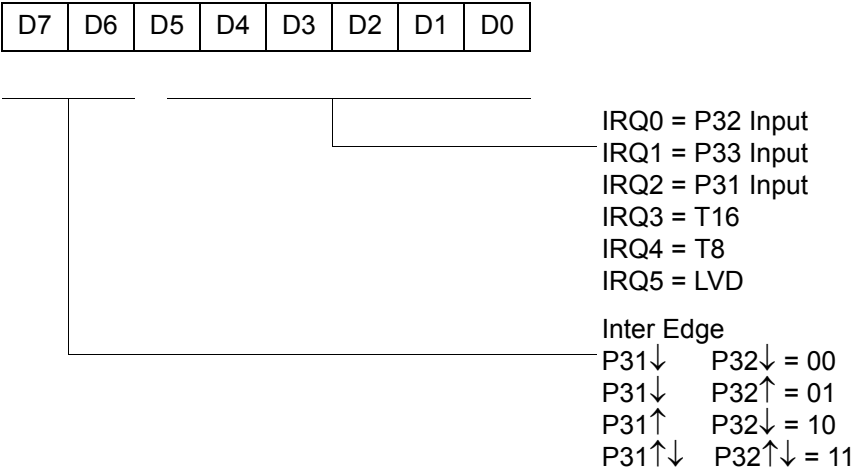


Figure 49. Interrupt Request Register (FAH: Read/Write)

R251 IMR (FBH)



* Default setting after reset
** Only by using EI, DI instruction; DI is required before changing the IMR register

Figure 50. Interrupt Mask Register (FBH: Read/Write)



R252 Flags (FCH)

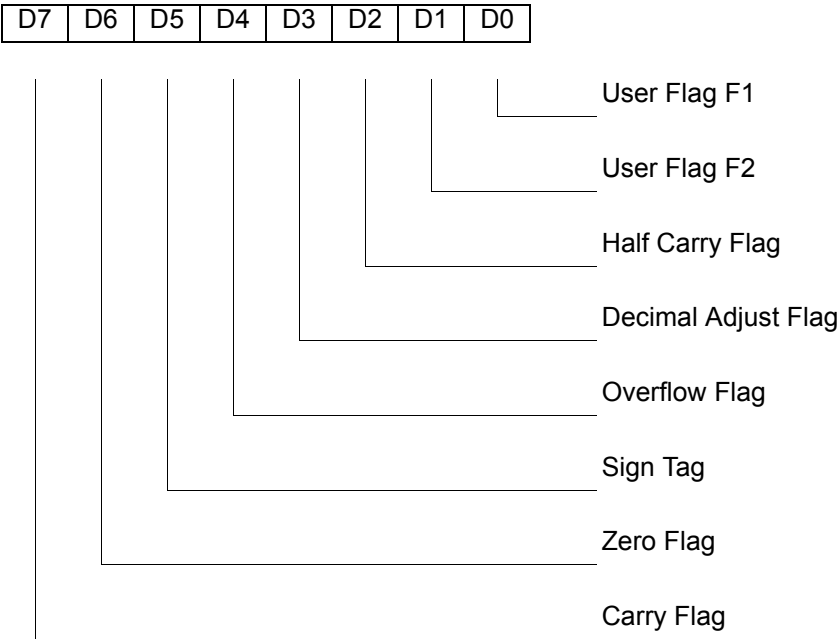
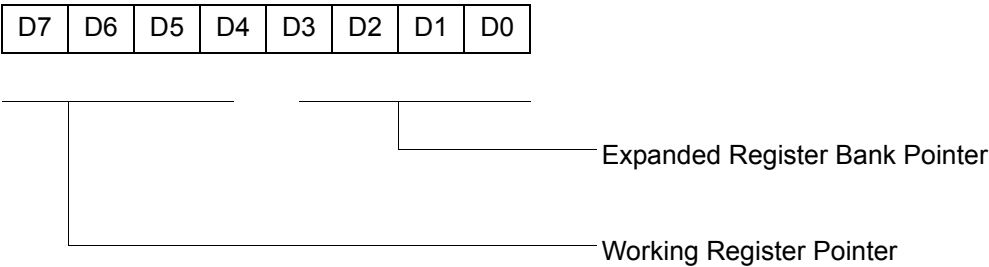


Figure 51. Flag Register (FCH: Read/Write)

R253 RP (FDH)



Default setting after reset = 0000 0000

Figure 52. Register Pointer (FDH: Read/Write)

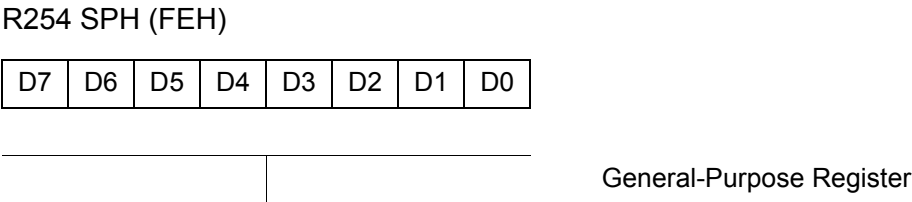


Figure 53. Stack Pointer High (FEH: Read/Write)

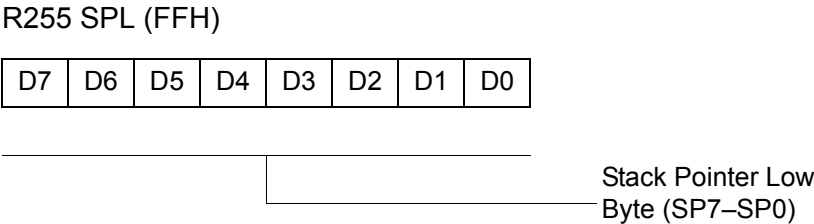
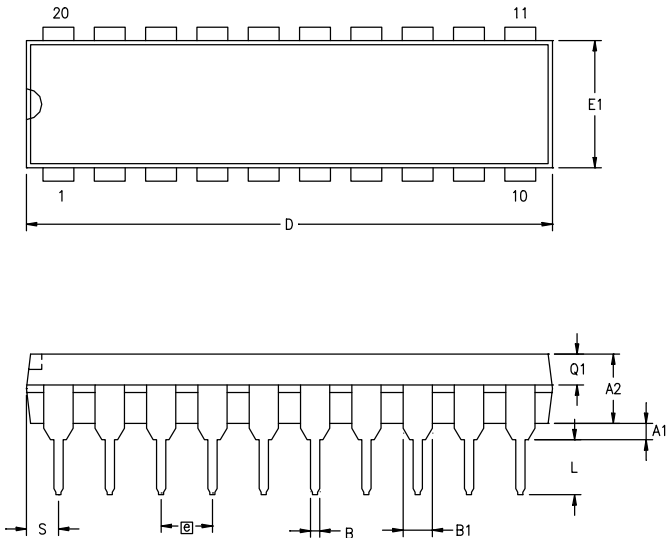


Figure 54. Stack Pointer Low (FFH: Read/Write)

Package Information

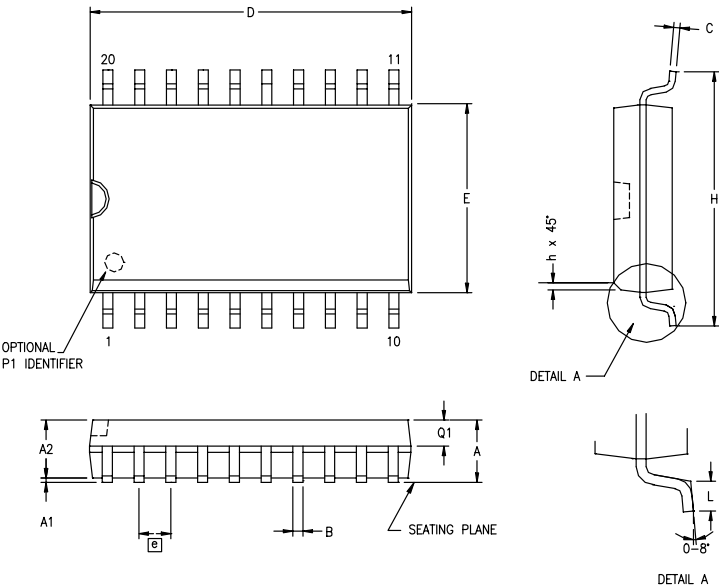
Package information for all device versions of ZGR16300 is depicted in Figures 55 through Figure 60.



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.38	0.81	.015	.032
A2	3.25	3.68	.128	.145
B	0.41	0.51	.016	.020
B1	1.47	1.57	.058	.062
C	0.20	0.30	.008	.012
D	25.65	26.16	1.010	1.030
E	7.49	8.26	.295	.325
E1	6.10	6.65	.240	.262
[G]	2.54 BSC		.100 BSC	
eA	7.87	9.14	.310	.360
L	3.18	3.43	.125	.135
Q1	1.42	1.65	.056	.065
S	1.52	1.65	.060	.065

CONTROLLING DIMENSIONS : INCH

Figure 55. 20-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	12.60	12.95	.496	.510
E	7.40	7.60	.291	.299
[G]	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 56. 20-Pin SOIC Package Diagram

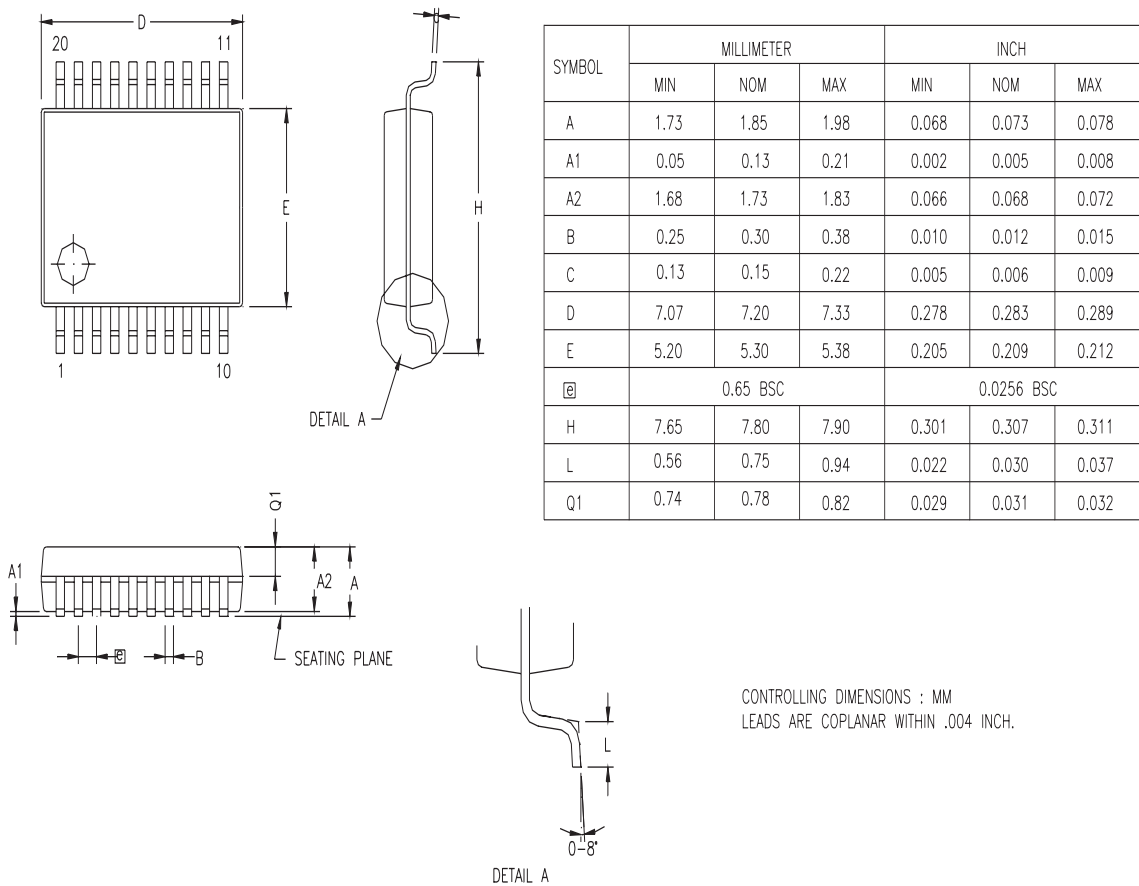
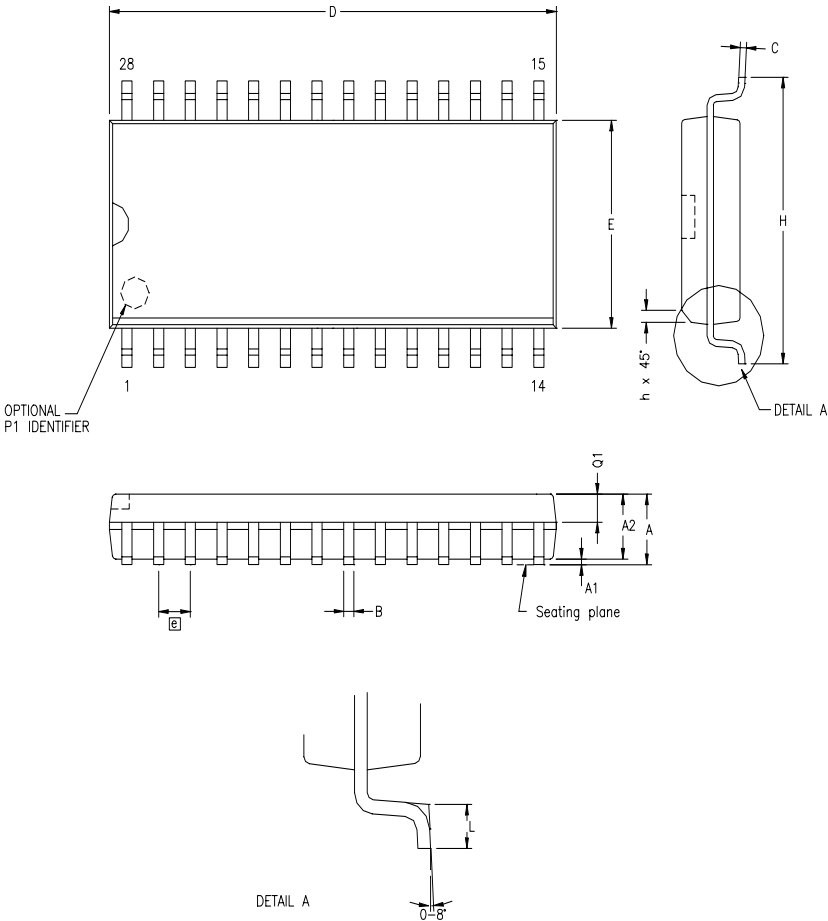


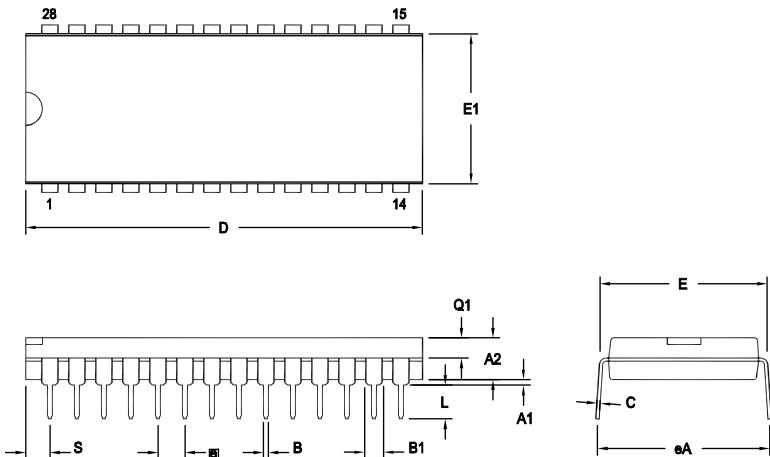
Figure 57. 20-Pin SSOP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
Ⓜ	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.09	.038	.043

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 58. 28-Pin SOIC Package Diagram



OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

Note: ZILOG supplies both options for production. Component layout
PCB design should cover bigger option 01.

SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.38	1.02	.015	.040
A2		3.18	4.19	.125	.165
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 BSC	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.40	1.91	.055	.075
	02	1.40	1.78	.055	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

CONTROLLING DIMENSIONS : INCH

Figure 59. 28-Pin DIP Package Diagram

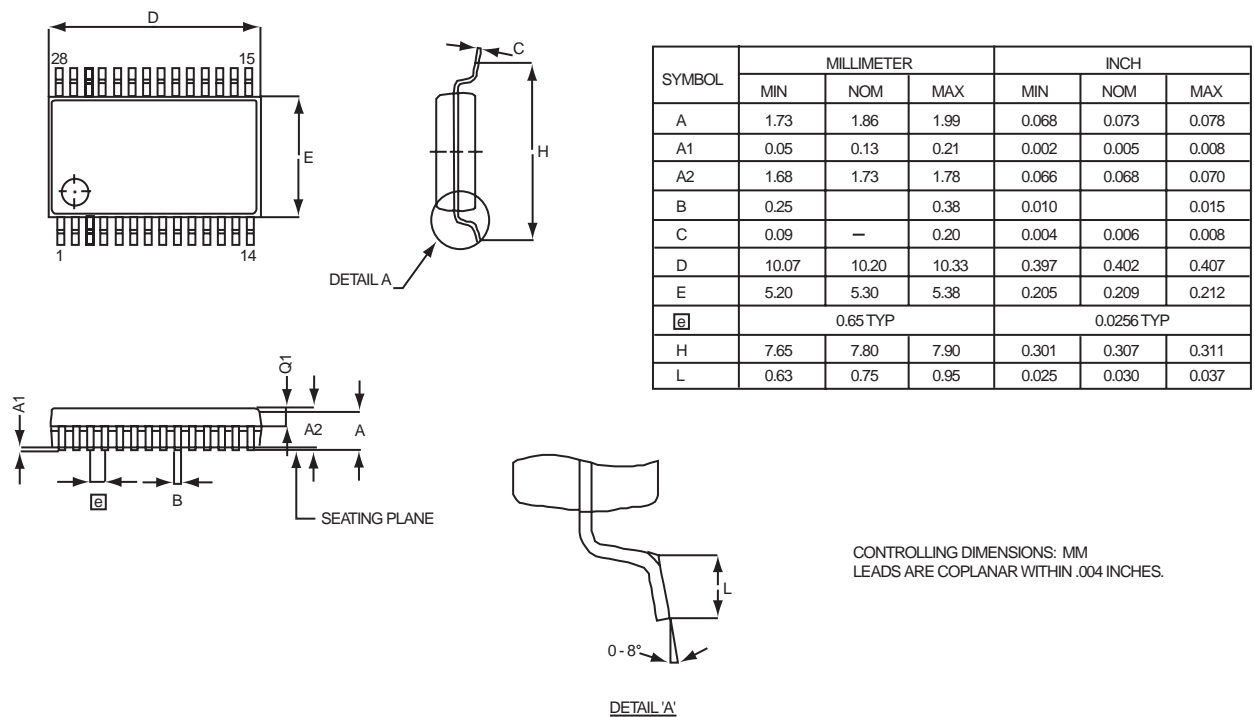


Figure 60. 28-Pin SSOP Package Diagram

► **Note:** Please check with ZiLOG® on the actual bonding diagram and coordinate for chip-on-board assembly.

Ordering Information

The following table provides ordering information for the ZLR16300 16K, 8K, 4K, 2K, and 1K parts.



Memory Size	Part No.	Description
16K	ZLR16300H2816C	28-pin SSOP 16K ROM
	ZLR16300P2816C	28-pin PDIP 16K ROM
	ZLR16300S2816C	28-pin SOIC 16K ROM
	ZLR16300H2016C	20-pin SSOP 16K ROM
	ZLR16300P2016C	20-pin PDIP 16K ROM
	ZLR16300S2016C	20-pin SOIC 16K ROM
8K	ZLR16300H2808C	28-pin SSOP 8K ROM
	ZLR16300P2808C	28-pin PDIP 8K ROM
	ZLR16300S2808C	28-pin SOIC 8K ROM
	ZLR16300H2008C	20-pin SSOP 8K ROM
	ZLR16300P2008C	20-pin PDIP 8K ROM
	ZLR16300S2008C	20-pin SOIC 8K ROM
4K	ZLR16300H2804C	28-pin SSOP 4K ROM
	ZLR16300P2804C	28-pin PDIP 4K ROM
	ZLR16300S2804C	28-pin SOIC 4K ROM
	ZLR16300H2004C	20-pin SSOP 4K ROM
	ZLR16300P2004C	20-pin PDIP 4K ROM
	ZLR16300S2004C	20-pin SOIC 4K ROM
2K	ZLR16300H2802C	28-pin SSOP 2K ROM
	ZLR16300P2802C	28-pin PDIP 2K ROM
	ZLR16300S2802C	28-pin SOIC 2K ROM
	ZLR16300H2002C	20-pin SSOP 2K ROM
	ZLR16300P2002C	20-pin PDIP 2K ROM
	ZLR16300S2002C	20-pin SOIC 2K ROM
1K	ZLR16300H2801C	28-pin SSOP 1K ROM
	ZLR16300P2801C	28-pin PDIP 1K ROM
	ZLR16300S2801C	28-pin SOIC 1K ROM
	ZLR16300H2001C	20-pin SSOP 1K ROM
	ZLR16300P2001C	20-pin PDIP 1K ROM
	ZLR16300S2001C	20-pin SOIC 1K ROM
	ZLP32300100KIT	Development System
	ZLP323ICE01ZEM	Emulator

Note:

1. Replace C with G for Lead-Free Packaging.
2. Contact www.zilog.com for the die form.



For fast results, contact your local ZiLOG sales office for assistance in ordering the part desired.

Codes

ZL = ZiLOG Low Voltage Family

R = ROM

16300 = Family Designation

P = Package Type:

H = SSOP

P = Plastic DIP

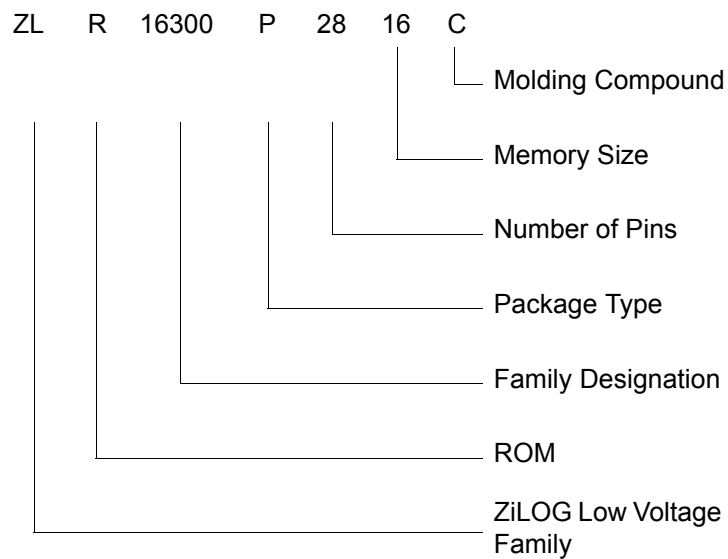
S = SOIC

= Number of Pins

CC = Memory Size

X = Molding Compound

Example





Index

Numerics

- 16-bit counter/timer circuits 39
- 20-pin DIP package diagram 74
- 20-pin SSOP package diagram 75
- 28-pin DIP package diagram 77
- 28-pin SOIC package diagram 76
- 28-pin SSOP package diagram 78
- 8-bit counter/timer circuits 35

A

- absolute maximum ratings 6
- AC
 - characteristics 10
 - timing diagram 10
- address spaces, basic 2
- architecture 2
 - expanded register file 21

B

- basic address spaces 2
- block diagram, ZLR16300 functional 3

C

- capacitance 8
- capture_INT_mask 27, 32
- characteristics
 - AC 10
 - DC 8
- clock 46
- comparator inputs/outputs 18
- configuration
 - port 0 13
 - port 2 14
 - port 3 15
 - port 3 counter/timer 17
- counter/timer
 - 16-bit circuits 39

- 8-bit circuits 35
- brown-out voltage/standby 57
- clock 46
- demodulation mode count capture flow-chart 37
- demodulation mode flowchart 38
- EPROM selectable options 57
- glitch filter circuitry 33
- halt instruction 47
- input circuit 33
- interrupt block diagram 44
- interrupt types, sources and vectors 45
- oscillator configuration 46
- output circuit 42
- ping-pong mode 41
- port configuration register 48
- resets and WDT 56
- SCLK circuit 51
- stop instruction 47
- stop mode recovery register 50
- stop mode recovery register 2 54
- stop mode recovery source 52
- T16 demodulation mode 40
- T16 transmit mode 39
- T16_OUT in modulo-N mode 40
- T16_OUT in single-pass mode 40
- T8 demodulation mode 36
- T8 transmit mode 33
- T8_OUT in modulo-N mode 36
- T8_OUT in single-pass mode 36
- transmit mode flowchart 34
- voltage detection and flags 58
- watch-dog timer mode register 55
- watch-dog timer time select 56
- counter/timer functional blocks
 - input circuit 33
 - T8 transmit mode 33
- counter_INT_mask 32
- crt3 T8/T16 control register
 - register 32



CTR(D)01h T8 and T16 common functions 28
 CTR1 (0D)01 27
 CTR3 T8/T16 control CTR3(0D)03h 32

D

DC characteristics 8
 demodulation mode
 count capture flowchart 37
 flowchart 38
 T16 40
 T8 36
 description
 functional 18
 general 2
 pin 5

E

EPROM
 selectable options 57
 expanded register file 20
 expanded register file architecture 21
 expanded register file control registers 63
 flag 72
 interrupt mask register 71
 interrupt priority register 70
 interrupt request register 71
 port 0 and 1 mode register 69
 port 2 configuration register 67
 port 3 mode register 68
 port configuration register 67
 register pointer 72
 stack pointer high register 73
 stack pointer low register 73
 stop-mode recovery register 65
 stop-mode recovery register 2 66
 T16 control register 61
 T8 and T16 common control functions register 60
 TC8 control register 58
 watch-dog timer register 67

F

features
 standby modes 1
 ZLR16300 1
 functional description
 counter/timer functional blocks 33
 CTR0(0D)00h register 26
 CTR1(0D)01h register 28
 CTR2(0D)02h register 30
 expanded register file 20
 expanded register file architecture 21
 HI16(0D)09h register 25
 HI8(0D)0Bh register 25
 L08(0D)0Ah register 25
 L0I6(0D)08h register 25
 program memory map 19
 RAM 18
 register description 57
 register file 23
 register pointer 22
 register pointer detail 24
 stack 24
 TC16H(0D)07h register 25
 TC16L(0D)06h register 26
 TC8H(0D)05h register 26
 TC8L(0D)04h register 26
 TC8L(D)04h register 26

G

glitch filter circuitry 33

H

halt instruction, counter/timer 47

I

input circuit 33
 interrupt block diagram, counter/timer 44
 interrupt types, sources and vectors 45



L

low-voltage detection register 57

M

memory, program 18

modulo-N mode

 T16_OUT 40

 T8_OUT 36

O

oscillator configuration 46

output circuit, counter/timer 42

P

P34_out 27

P35_out 32

P36_out/demodulator input 29

package information

 20-pin DIP package diagram 74

 20-pin SSOP package diagram 75

 28-pin DIP package diagram 77

 28-pin SOIC package diagram 76

 28-pin SSOP package diagram 78

pin configuration

 20-pin DIP/SOIC/SSOP 5

 28-pin DIP/SOIC/SSOP 6

pin functions

 port 0 (P07 - P00) 12

 port 0 configuration 13

 port 2 (P27 - P20) 13

 port 2 (P37 - P30) 14

 port 2 configuration 14

 port 3 configuration 15

 port 3 counter/timer configuration 17

 XTAL1 (time-based input) 12

 XTAL2 (time-based output) 12

ping-pong mode 41

port 0

 configuration 13

 pin function 12

port 2

 configuration 14

 pin function 13

port 3

 configuration 15

 counter/timer configuration 17

port 3 pin function 14

port configuration register 48

power connections 2

power supply 5

program memory 18

 map 19

R

ratings, absolute maximum 6

register 54

 CTR0(0D)00h 26

 CTR1 (0D) 01 27

 CTR1(0D)01h 28

 CTR2(0D)02h 30

 flag 72

 HI16(0D)09h 25

 HI8(0D)0Bh 25

 interrupt priority 70

 interrupt request 71

 interruptmask 71

 L016(0D)08h 25

 L08(0D)0Ah 25

 LVD(D)0Ch 57

 pointer 72

 port 0 and 1 69

 port 2 configuration 67

 port 3 mode 68

 port configuration 48, 67

 stack pointer high 73

 stack pointer low 73

 stop mode recovery 50

 stop mode recovery 2 54

 stop-mode recovery 65

 stop-mode recovery 2 66

 T16 control 61

 T8 and T16 common control functions 60

 TC16H(0D)07h 25



- TC16L(0D)06h 26
- TC8 control 58
- TC8H(0D)05h 26
- TC8L(0D)04h 26
- TC8L(D)04h 26
- voltage detection 63
- watch-dog timer 67
- register description
 - counter/timer2 LS-Byte hold 26
 - counter/timer2 MS-Byte hold 25
 - counter/timer8 control 26
 - counter/timer8 High hold 26
 - counter/timer8 Low hold 26
 - CTR2 counter/timer 16 control 30
 - T16_capture_LO 25
 - T8 and T16 common functions 28
 - T8_Capture_HI 25
 - T8_capture_LO 25
- register file 23
 - expanded 20
- register pointer 22
 - detail 24
- resets and WDT 56

S

- SCLK circuit 51
- single/modulo-N 27, 31
- single-pass mode
 - T16_OUT 40
 - T8_OUT 36
- stack 24
- standard test conditions 7
- standby modes 1
- stop instruction, counter/timer 47
- stop mode recovery
 - 2 register 54
 - source 52
- stop mode recovery 2 54
- stop mode recovery register 50

T

- T 16 clock 32
- T16 enable 31
- T16 initial out/falling edge 30
- T16 transmit mode 39
- T16_capture_HI 25
- T8 and T16 common functions 27
- t8 clock 27
- T8 enable 27
- T8 initial out/rising edge 30
- T8 transmit mode 33
- T8/T16_logic/edge_detect 30
- T8_Capture_HI 25
- test conditions, standard 7
- test load diagram 7
- time_out 32
- timeout 27
- timers
 - counter/timer2 LS-byte hold 26
 - counter/timer2 MS-byte hold 25
 - counter/timer8 high hold 26
 - counter/timer8 low hold 26
 - CTR0 counter/timer8 control 26
 - T16_Capture_HI 25
 - T16_Capture_LO 25
 - T8_Capture_HI 25
 - T8_Capture_LO 25
- timing diagram, AC 10
- transmit mode flowchart 34
- transmit_submode/glitch filter 30

V

- VCC 5
- voltage
 - brown-out/standby 57
 - detection and flags 58
- voltage detection register 63



W

watch-dog timer
mode registerwatch-dog timer mode register 55
time select 56

X

XTAL1 5
XTAL1 pin function 12
XTAL2 5
XTAL2 pin function 12

Z

ZLR16300 family members 1