



Crimzon™ ZLR32300

***Z8 Low-Voltage ROM
MCU with Infrared Timers***

Product Specification

PS022607-1205



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Revision History

Each instance in [Table 1](#) reflects a change to this document from its previous revision. To see more detail, click the appropriate link in the table.

Table 1. Revision History of this Document

Date	Revision Level	Description	Page #
January 2005	03	Added characterization data, modified Table 8.	1, 2, 11, 12
		Removed Preliminary designation	All
April 2005	04	Clarified functioning of Port 1 in 20 and 28-packaging. Closes CR5842.	16, 25
May 2005	05	Updated Ordering Information on page 85 .	
August 2005	06	Removed the 40-pin package. Added caution to Input/Output Ports on page 14 . Updated Ordering Information on page 85 .	
December 2005	07	Updated section clock and Input/output port	50, 14



Table of Contents

Revision History	iii
Development Features	1
General Description	2
Pin Description	4
Absolute Maximum Ratings	9
Standard Test Conditions	9
DC Characteristics	10
AC Characteristics	12
Pin Functions	14
XTAL1 Crystal 1 (Time-Based Input)	14
XTAL2 Crystal 2 (Time-Based Output)	14
Input/Output Ports	14
RESET (Input, Active Low)	22
Functional Description	22
Program Memory	22
RAM	22
Expanded Register File	23
Register File	27
Stack	28
Timers	29
Counter/Timer Functional Blocks	37
Interrupts	47
Clock	50
Power Management	51
Port Configuration	52
Stop-Mode Recovery	53
Watch-Dog Timer Mode	59
Low-Voltage Detection	62
Expanded Register File Control Registers (0D)	63
Expanded Register File Control Registers (0F)	68
Standard Control Registers	72
Package Information	78
Ordering Information	85



Part Number Description 86



List of Figures

Figure 1. Functional Block Diagram	3
Figure 2. Counter/Timers Diagram	4
Figure 3. 20-Pin PDIP/SOIC/SSOP Pin Configuration	5
Figure 4. 28-Pin PDIP/SOIC/SSOP Pin Configuration	6
Figure 5. 48-Pin SSOP Pin Configuration	7
Figure 6. Test Load Diagram	9
Figure 7. AC Timing Diagram	12
Figure 8. Port 0 Configuration	16
Figure 9. Port 1 Configuration	17
Figure 10. Port 2 Configuration	18
Figure 11. Port 3 Configuration	19
Figure 12. Port 3 Counter/Timer Output Configuration	21
Figure 13. Program Memory Map (32K ROM)	23
Figure 14. Expanded Register File Architecture	25
Figure 15. Register Pointer	26
Figure 16. Register Pointer—Detail	28
Figure 17. Glitch Filter Circuitry	37
Figure 18. Transmit Mode Flowchart	38
Figure 19. 8-Bit Counter/Timer Circuits	39
Figure 20. T8_OUT in Single-Pass Mode	40
Figure 21. T8_OUT in Modulo-N Mode	40
Figure 22. Demodulation Mode Count Capture Flowchart	41
Figure 23. Demodulation Mode Flowchart	42
Figure 24. 16-Bit Counter/Timer Circuits	43
Figure 25. T16_OUT in Single-Pass Mode	44
Figure 26. T16_OUT in Modulo-N Mode	44
Figure 27. Ping-Pong Mode Diagram	46
Figure 28. Output Circuit	46
Figure 29. Interrupt Block Diagram	48
Figure 30. Oscillator Configuration	50
Figure 31. Port Configuration Register (PCON) (Write Only)	52
Figure 32. STOP Mode Recovery Register	54
Figure 33. SCLK Circuit	55
Figure 34. STOP Mode Recovery Source	56



Figure 35. STOP Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only)	58
Figure 36. WATCH-DOG TIMER Mode Register (Write Only)	59
Figure 37. Resets and WDT	61
Figure 38. TC8 Control Register ((0D)00H: Read/Write Except Where Noted)	64
Figure 39. T8 and T16 Common Control Functions ((0D)01H: Read/Write)	65
Figure 40. T16 Control Register ((0D) 2H: Read/Write Except Where Noted)	66
Figure 41. T8/T16 Control Register (0D)03H: Read/Write (Except Where Noted)	67
Figure 42. Voltage Detection Register	68
Figure 43. Port Configuration Register (PCON)(0F)00H: Write Only)	69
Figure 44. STOP mode Recovery Register ((0F)0BH: D6–D0=Write Only, D7=Read Only)	70
Figure 45. STOP mode Recovery Register 2 ((0F)0DH:D2–D4, D6 Write Only)	71
Figure 46. Watch-Dog Timer Register ((0F) 0FH: Write Only)	72
Figure 47. Port 2 Mode Register (F6H: Write Only)	72
Figure 48. Port 3 Mode Register (F7H: Write Only)	73
Figure 49. Port 0 and 1 Mode Register (F8H: Write Only)	74
Figure 50. Interrupt Priority Register (F9H: Write Only)	75
Figure 51. Interrupt Request Register (FAH: Read/Write)	76
Figure 52. Interrupt Mask Register (FBH: Read/Write)	76
Figure 53. Flag Register (FCH: Read/Write)	77
Figure 54. Register Pointer (FDH: Read/Write)	77
Figure 55. Stack Pointer High (FEH: Read/Write)	78
Figure 56. Stack Pointer Low (FFH: Read/Write)	78
Figure 57. 20-Pin PDIP Package Diagram	79
Figure 58. 20-Pin SOIC Package Diagram	79
Figure 59. 20-Pin SSOP Package Diagram	80
Figure 60. 28-Pin SOIC Package Diagram	81
Figure 61. 28-Pin PDIP Package Diagram	82
Figure 62. 28-Pin SSOP Package Diagram	83
Figure 63. 48-Pin SSOP Package Design	84
Figure 64. Part Number Description Example	86



List of Tables

Table 1.	Revision History of this Document	iii
Table 2.	Features	1
Table 3.	Power Connections	2
Table 4.	20-Pin PDIP/SOIC/SSOP Pin Identification	5
Table 5.	28-Pin PDIP/SOIC/SSOP Pin Identification	6
Table 6.	48- Pin Configuration	7
Table 7.	Absolute Maximum Ratings	9
Table 8.	Capacitance	10
Table 9.	LR32300 DC Characteristics	10
Table 10.	AC Characteristics	13
Table 11.	Port 3 Pin Function Summary	20
Table 12.	CTR0(D)00H Counter/Timer8 Control Register	30
Table 13.	CTR1(0D)01H T8 and T16 Common Functions	32
Table 14.	CTR2(D)02H: Counter/Timer16 Control Register	35
Table 15.	CTR3 (D)03H: T8/T16 Control Register	36
Table 16.	Interrupt Types, Sources, and Vectors	49
Table 17.	IRQ Register	49
Table 18.	SMR2(F)0Dh:STOP mode Recovery Register 2*	55
Table 19.	STOP Mode Recovery Source	57
Table 20.	Watch-Dog Timer Time Select	60
Table 21.	ROM Selectable Options	62

Development Features

Table 2 lists the features of ZiLOG®'s Crimzon™ ZLR32300 family members.

Table 2. Features

Device	ROM (KB)	RAM* (Bytes)	I/O Lines	Voltage Range
Crimzon™ ZLR32300	4, 8, 16, 24, 32	237	32, 24 or 16	2.0V–3.6V
Note: *General purpose				

- Low power consumption—5 mW (typical)
- Three standby modes:
 - STOP—1.4µA (typical)
 - HALT—0.5mA (typical)
 - Low voltage
- Special architecture to automate both generation and reception of complex pulses or signals:
 - One programmable 8-bit counter/timer with two capture registers and two load registers
 - One programmable 16-bit counter/timer with one 16-bit capture register pair and one 16-bit load register pair
 - Programmable input glitch filter for pulse reception
- Six priority interrupts
 - Three external
 - Two assigned to counter/timers
 - One low-voltage detection interrupt
- Low voltage detection and high voltage detection flags
- Programmable Watch-Dog Timer/Power-On Reset (WDT/POR) circuits
- Two independent comparators with programmable interrupt polarity
- Mask selectable pull-up transistors on ports 0, 1, 2, 3
- ROM options
 - Port 0: 0–3 pull-up transistors
 - Port 0: 4–7 pull-up transistors
 - Port 1: 0–3 pull-up transistors
 - Port 1: 4–7 pull-up transistors
 - Port 2: 0–7 pull-up transistors

- Port 3: 0–3 pull-up transistors
- WDT enabled at POR

General Description

The Crimzon™ ZLR32300 is an ROM-based member of the MCU family of infra-red microcontrollers. With 237B of general-purpose RAM and 4KB to 32KB of ROM, ZiLOG®'s CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The Crimzon™ ZLR32300 architecture ([Figure 1](#)) is based on ZiLOG's 8-bit microcontroller core with an Expanded Register File allowing access to register-mapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8® offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations: Program Memory, Register File and Expanded Register File. The register file is composed of 256 Bytes (B) of RAM. It includes 4 I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

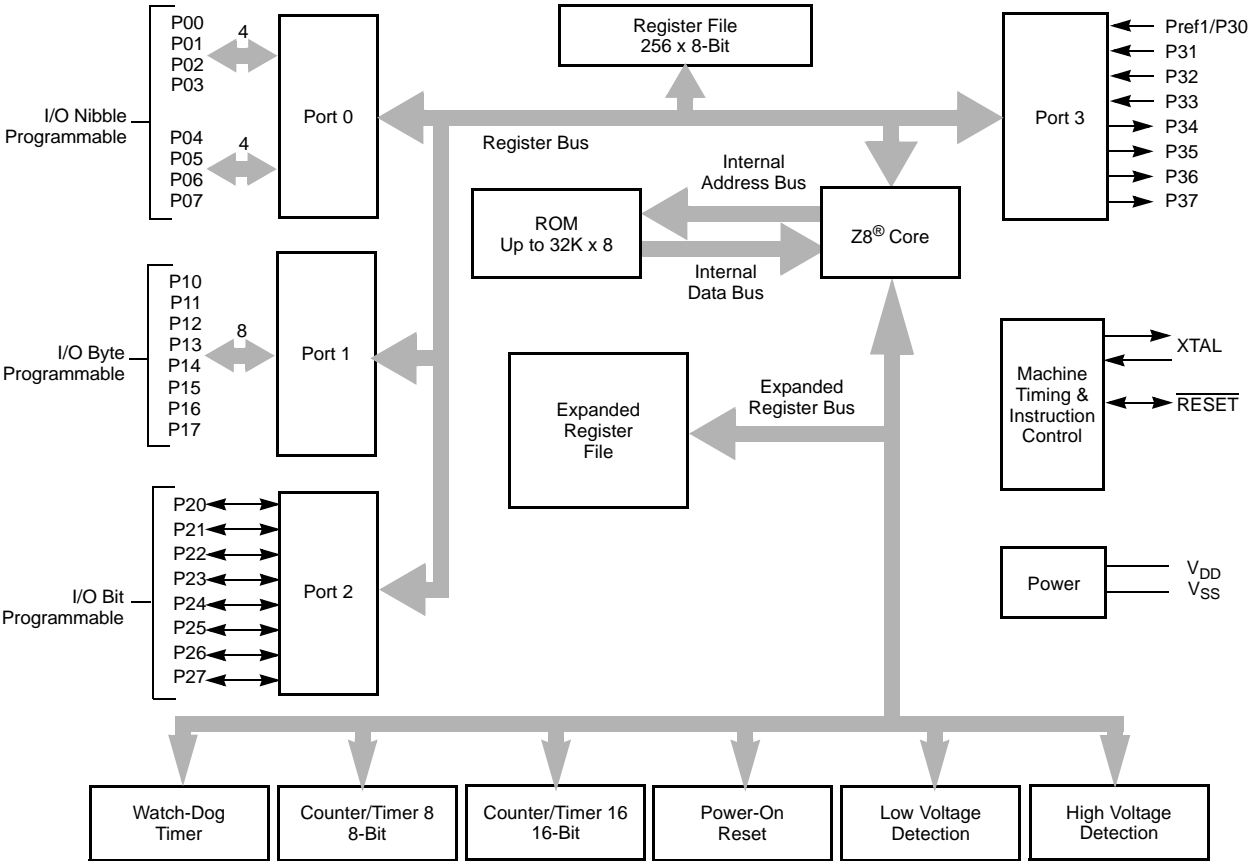
To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Crimzon™ ZLR32300 offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see [Figure 2](#)). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages.

► **Note:** All signals with an overline, “ $\overline{}$ ”, are active Low. For example, $\overline{B/W}$, in which WORD is active Low, and $\overline{B/W}$, in which BYTE is active Low.

Power connections use the conventional descriptions listed in [Table 3](#).

Table 3. Power Connections

Connection	Circuit	Device
Power	V _{CC}	V _{DD}
Ground	GND	V _{SS}



Note: Refer to the specific package for available pins.

Figure 1. Functional Block Diagram

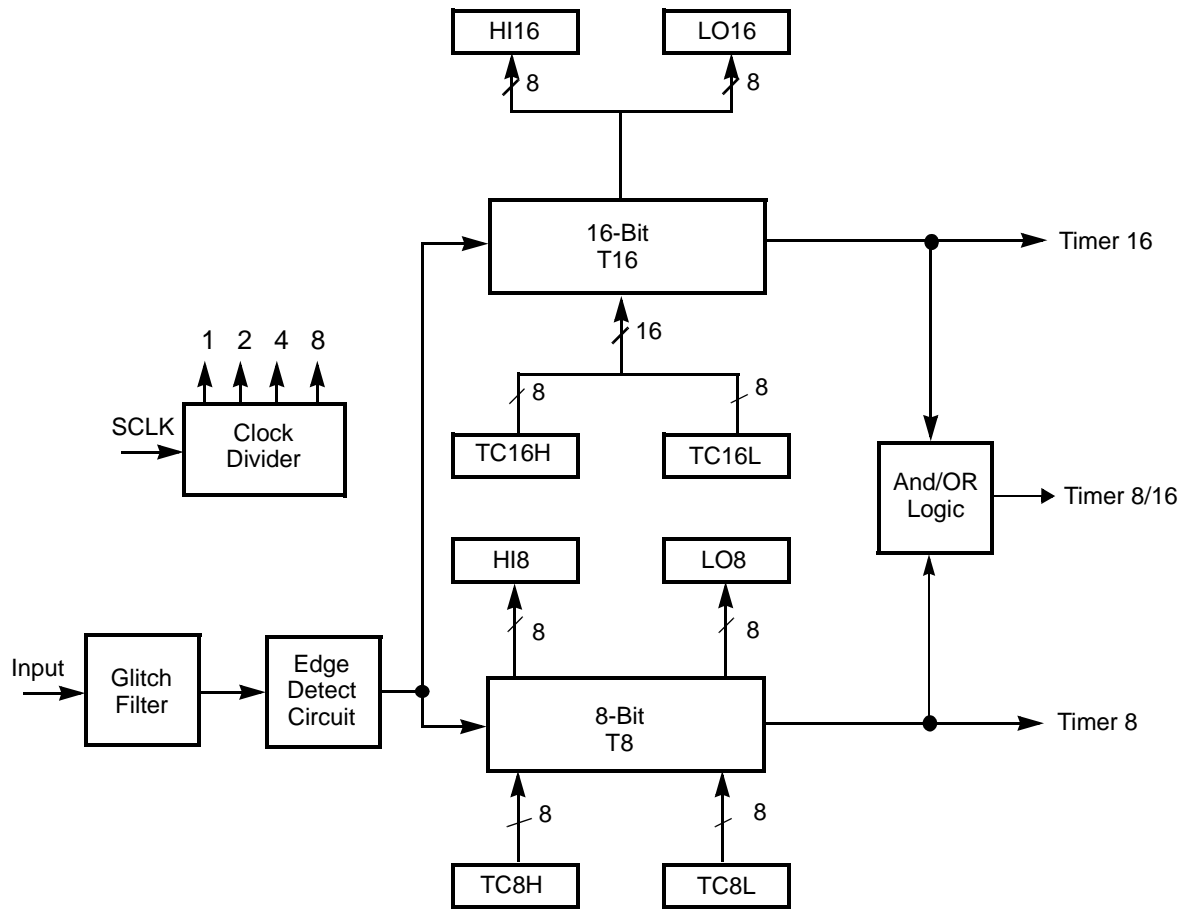


Figure 2. Counter/Timers Diagram

Pin Description

The pin configuration for the 20-pin PDIP/SOIC/SSOP is illustrated in [Figure 3](#) and described in [Table 4](#). The pin configuration for the 28-pin DIP/SOIC/SSOP are depicted in [Figure 4](#) and described in [Table 5](#). The pin configurations for the 48-pin SSOC versions are illustrated in [Figure 5](#) and described in [Table 6](#).

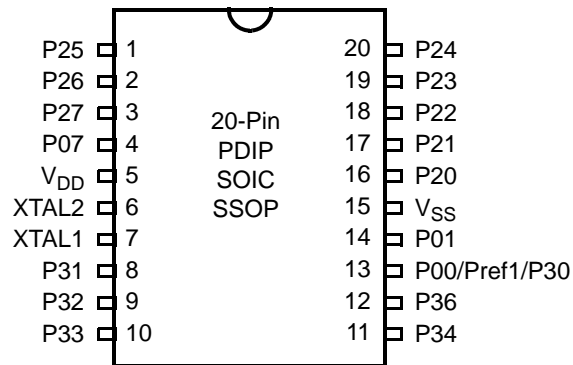


Figure 3. 20-Pin PDIP/SOIC/SSOP Pin Configuration

Table 4. 20-Pin PDIP/SOIC/SSOP Pin Identification

Pin #	Symbol	Function	Direction
1–3	P25–P27	Port 2, Bits 5,6,7	Input/Output
4	P07	Port 0, Bit 7	Input/Output
5	V _{DD}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8–10	P31–P33	Port 3, Bits 1,2,3	Input
11,12	P34, P36	Port 3, Bits 4,6	Output
13	P00/Pref1/P30	Port 0, Bit 0/Analog reference input Port 3 Bit 0	Input/Output for P00 Input for Pref1/P30
14	P01	Port 0, Bit 1	Input/Output
15	V _{SS}	Ground	
16–20	P20–P24	Port 2, Bits 0,1,2,3,4	Input/Output

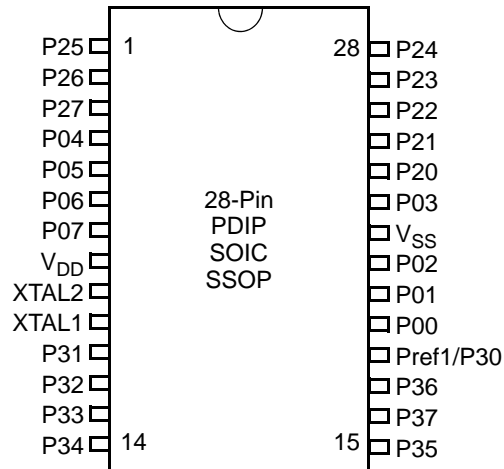


Figure 4. 28-Pin PDIP/SOIC/SSOP Pin Configuration

Table 5. 28-Pin PDIP/SOIC/SSOP Pin Identification

Pin	Symbol	Direction	Description
1-3	P25-P27	Input/Output	Port 2, Bits 5,6,7
4-7	P04-P07	Input/Output	Port 0, Bits 4,5,6,7
8	V _{DD}		Power supply
9	XTAL2	Output	Crystal, oscillator clock
10	XTAL1	Input	Crystal, oscillator clock
11-13	P31-P33	Input	Port 3, Bits 1,2,3
14	P34	Output	Port 3, Bit 4
15	P35	Output	Port 3, Bit 5
16	P37	Output	Port 3, Bit 7
17	P36	Output	Port 3, Bit 6
18	Pref1/P30 Port 3 Bit 0	Input	Analog ref input; connect to V _{CC} if not used Input for Pref1/P30
19-21	P00-P02	Input/Output	Port 0, Bits 0,1,2
22	V _{SS}		Ground
23	P03	Input/Output	Port 0, Bit 3
24-28	P20-P24	Input/Output	Port 2, Bits 0-4

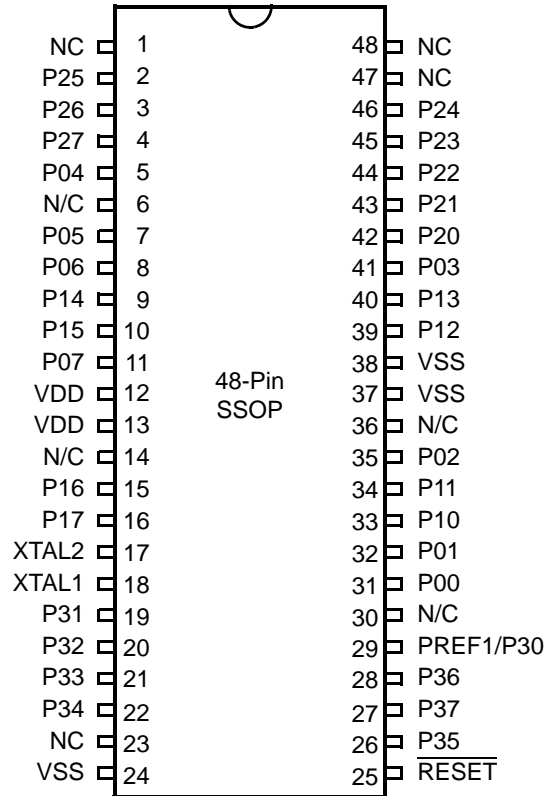


Figure 5. 48-Pin SSOP Pin Configuration

Table 6. 48- Pin Configuration

48-Pin SSOP #	Symbol
31	P00
32	P01
35	P02
41	P03
5	P04
7	P05
8	P06
11	P07
33	P10
34	P11
39	P12

Table 6. 48- Pin Configuration

48-Pin SSOP #	Symbol
40	P13
9	P14
10	P15
15	P16
16	P17
42	P20
43	P21
44	P22
45	P23
46	P24
2	P25
3	P26
4	P27
19	P31
20	P32
21	P33
22	P34
26	P35
28	P36
27	P37
23	NC
47	NC
1	NC
25	RESET
18	XTAL1
17	XTAL2
12, 13	V _{DD}
24, 37, 38	V _{SS}
29	Pref1/P30
48	NC
6	NC
14	NC
30	NC
36	NC



Absolute Maximum Ratings

Stresses greater than those listed in [Table 8](#) might cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period might affect device reliability.

Table 7. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units	Notes
Ambient temperature under bias	0	+70	C	
Storage temperature	-65	+150	C	
Voltage on any pin with respect to V_{SS}	-0.3	+4.0	V	1
Voltage on V_{DD} pin with respect to V_{SS}	-0.3	+3.6	V	
Maximum current on input and/or inactive output pin	-5	+5	μ A	
Maximum output current from active output pin	-25	+25	mA	
Maximum current into V_{DD} or out of V_{SS}		75	mA	

Notes:

1. This voltage applies to all pins except the following: V_{DD} and \overline{RESET} .

Standard Test Conditions

The characteristics listed in this product specification apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see [Figure 6](#)).

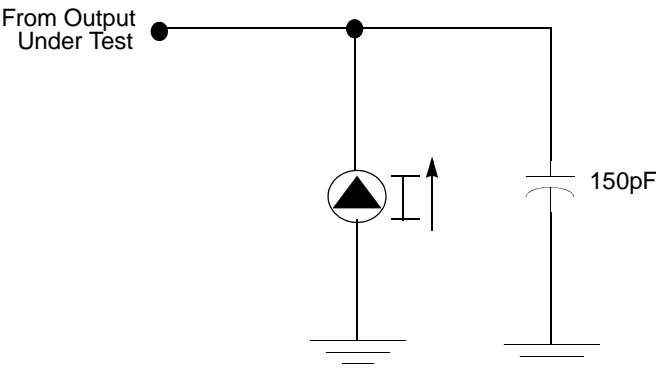


Figure 6. Test Load Diagram

Capacitance

Table 8 lists the capacitances.

Table 8. Capacitance

Parameter	Maximum
Input capacitance	12pF
Output capacitance	12pF
I/O capacitance	12pF
Note: $T_A = 25^\circ\text{C}$, $V_{CC} = \text{GND} = 0\text{V}$, $f = 1.0\text{MHz}$, unmeasured pins returned to GND	

DC Characteristics

Table 9. LR32300 DC Characteristics

Symbol	Parameter	V_{CC}	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$			Units	Conditions	Notes
			Min	Typ(7)	Max			
V_{CC}	Supply Voltage		2.0		3.6	V	See Note 5	5
V_{CH}	Clock Input High Voltage	2.0-3.6	$0.8V_{CC}$		$V_{CC}+0.3$	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.0-3.6	$V_{SS}-0.3$		0.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0-3.6	$0.7V_{CC}$		$V_{CC}+0.3$	V		
V_{IL}	Input Low Voltage	2.0-3.6	$V_{SS}-0.3$		$0.2V_{CC}$	V		
V_{OH1}	Output High Voltage	2.0-3.6	$V_{CC}-0.4$			V	$I_{OH} = -0.5\text{mA}$	
V_{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-3.6	$V_{CC}-0.8$			V	$I_{OH} = -7\text{mA}$	
V_{OL1}	Output Low Voltage	2.0-3.6			0.4	V	$I_{OL} = 4.0\text{mA}$	
V_{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-3.6			0.8	V	$I_{OL} = 10\text{mA}$	
V_{OFFSET}	Comparator Input Offset Voltage	2.0-3.6			25	mV		
V_{REF}	Comparator Reference Voltage	2.0-3.6	0		$V_{DD}-1.75$	V		
I_{IL}	Input Leakage	2.0-3.6	-1		1	μA	$V_{IN} = 0\text{V}$, V_{CC} Pull-ups disabled	
R_{PU}	Pull-Up Resistance		225		675	K Ω	$V_{IN} = 0\text{V}$; Pullups selected by mask option	
			75		275	K Ω		
I_{OL}	Output Leakage	2.0-3.6	-1		1	μA	$V_{IN} = 0\text{V}$, V_{CC}	
I_{CC}	Supply Current	2.0		1.2	3	mA	at 8.0 MHz	1, 2
		3.6		2.2	5	mA	at 8.0 MHz	1, 2

Table 9. LR32300 DC Characteristics (Continued)

Symbol	Parameter	V _{CC}	T _A = 0°C to +70°C			Units	Conditions	Notes
			Min	Typ(7)	Max			
I _{CC1}	Standby Current (HALT Mode)	2.0		0.5	1.6	mA	V _{IN} = 0V, V _{CC} at 8.0MHz	1, 2, 6
		3.6		0.8	2.0	mA	Same as above	1, 2, 6
I _{CC2}	Standby Current (STOP mode)	2.0		1.5	8	μA	V _{IN} = 0 V, V _{CC} WDT is not Running	3
		3.6		2.1	10	μA	Same as above	3
		2.0		4.7	20	μA	V _{IN} = 0 V, V _{CC} WDT is Running	3
		3.6		7.4	30	μA	Same as above	3
I _{LV}	Standby Current (Low Voltage)			1.0	6	μA	Measured at 1.3V	4
V _{BO}	V _{CC} Low Voltage Protection			1.8	2.0	V	8MHz maximum Ext. CLK Freq.	
V _{LVD}	V _{CC} Low Voltage Detection			2.4		V		
V _{HVD}	V _{CC} High Voltage Detection			2.7		V		

Notes:

1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. Oscillator stopped.
4. Oscillator stops when V_{CC} falls below V_{BO} limit.
5. It is strongly recommended to add a filter capacitor (minimum 0.1 μF), physically close to VDD and GND if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.
6. Comparator and Timers are on. Interrupt disabled.
7. Typical values shown are at 25 degrees C.



AC Characteristics

Figure 7 and Table 10 describe the Alternating Current (AC) characteristics.

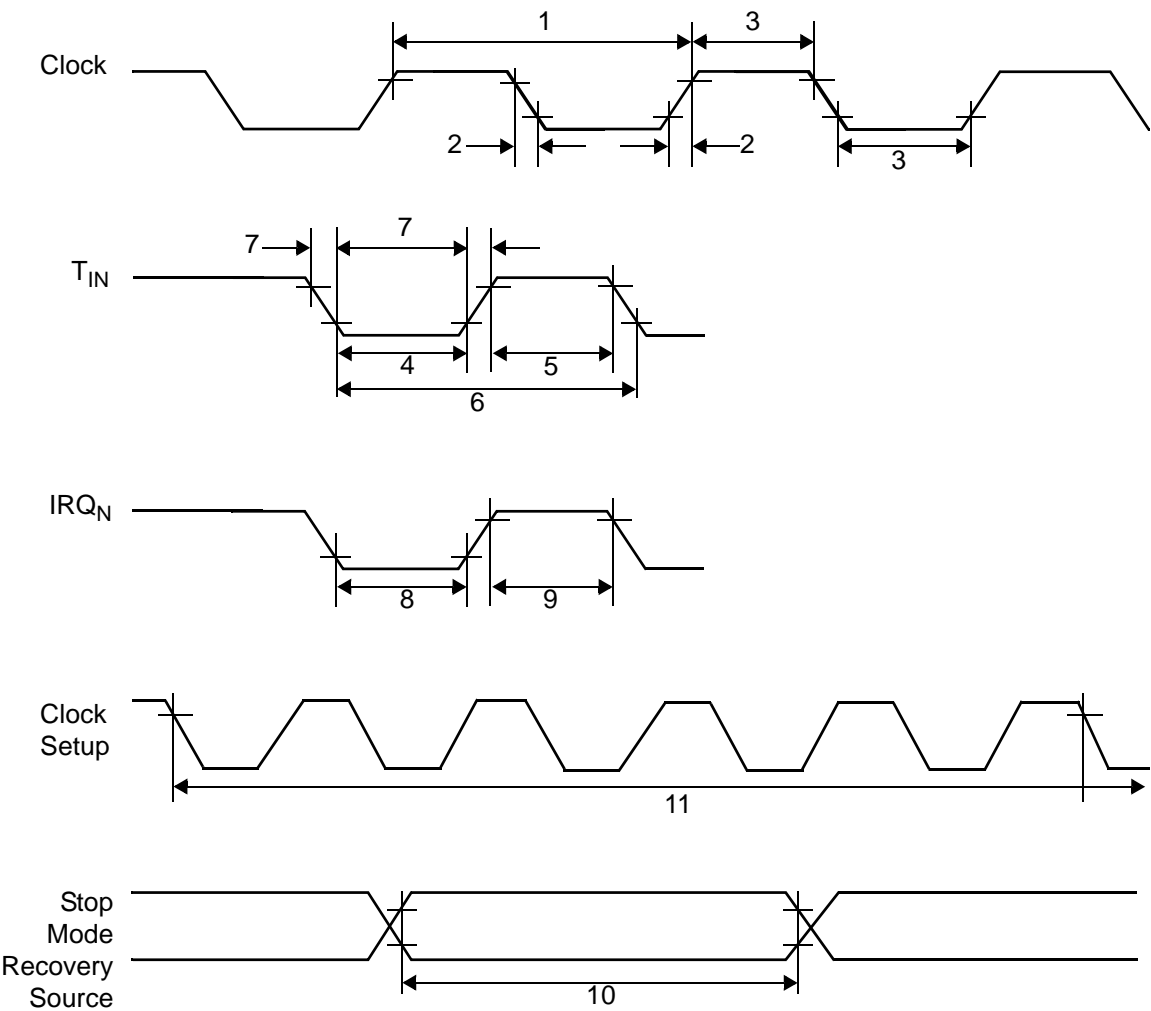


Figure 7. AC Timing Diagram



Table 10. AC Characteristics

T _A =0°C to +70°C 8.0MHz							Watch-Dog Timer Mode Register (D1, D0)
No	Symbol	Parameter	V _{CC}	Minimum	Maximum	Units	Notes
1	TpC	Input Clock Period	2.0–3.6	121	DC	ns	1
2	TrC, TfC	Clock Input Rise and Fall Times	2.0–3.6		25	ns	1
3	TwC	Input Clock Width	2.0–3.6	37		ns	1
4	TwTinL	Timer Input Low Width	2.0 3.6	100 70		ns	1
5	TwTinH	Timer Input High Width	2.0–3.6	3TpC			1
6	TpTin	Timer Input Period	2.0–3.6	8TpC			1
7	TrTin, TfTin	Timer Input Rise and Fall Timers	2.0–3.6		100	ns	1
8	TwIL	Interrupt Request Low Time	2.0 3.6	100 70		ns	1, 2
9	TwIH	Interrupt Request Input High Time	2.0–3.6	10TpC			1, 2
10	Twsm	Stop-Mode Recovery Width Spec	2.0–3.6	12 10TpC		ns	3 4
11	Tost	Oscillator Start-Up Time	2.0–3.6		5TpC		4
12	Twdt	Watch-Dog Timer Delay Time	2.0–3.6 2.0–3.6 2.0–3.6 2.0–3.6	10 20 40 160		ms ms ms ms	0, 0 0, 1 1, 0 1, 1
13	T _{POR}	Power-On Reset	2.0–3.6	2.5	10	ms	

Notes:

1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. SMR – D5 = 1.
4. SMR – D5 = 0.

Pin Functions

XTAL1 Crystal 1 (Time-Based Input)

This pin connects a parallel-resonant crystal or ceramic resonator, to the on-chip oscillator input. Additionally, an optional external single-phase clock can be coded to the on-chip oscillator input.

XTAL2 Crystal 2 (Time-Based Output)

This pin connects a parallel-resonant, crystal or ceramic resonant to the on-chip oscillator output.

Input/Output Ports



Caution: The CMOS input buffer for each port 0, 1, or 2 pin is always connected to the pin, even when the pin is configured as an output. If the pin is configured as an open-drain output and no external signal is applied, a High output state can cause the CMOS input buffer to float. This might lead to excessive leakage current of more than 100 μ A. To prevent this leakage, connect the pin to an external signal with a defined logic level or ensure its output state is Low, especially during STOP mode.

Internal pull-ups are disabled on any given pin or group of port pins when programmed into output mode.

Port 0, 1, and 2 have both input and output capability. The input logic is always present no matter whether the port is configured as input or output. When doing a READ instruction, the MCU reads the actual value at the input logic but not from the output buffer. In addition, the instructions of OR, AND, and XOR have the Read-Modify-Write sequence. The MCU first reads the port, and then modifies the value and load back to the port.

Precaution must be taken if the port is configured as open-drain output or if the port is driving any circuit that makes the voltage different from the desired output logic. For example, pins P00–P07 are not connected to anything else. If it is configured as open-drain output with output logic as



ONE, it is a floating port and reads back as ZERO. The following instruction sets P00-P07 all LOW.

```
AND P0, #F0
```

Port 0 (P07–P00)

Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port. The output drivers are push-pull or open-drain controlled by bit D2 in the PCON register.

If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. After a hardware reset, Port 0 is configured as an input port.

An optional pull-up transistor is available as a mask option on all Port 0 bits with nibble select.



Note: The Port 0 direction is reset to be input following an SMR.

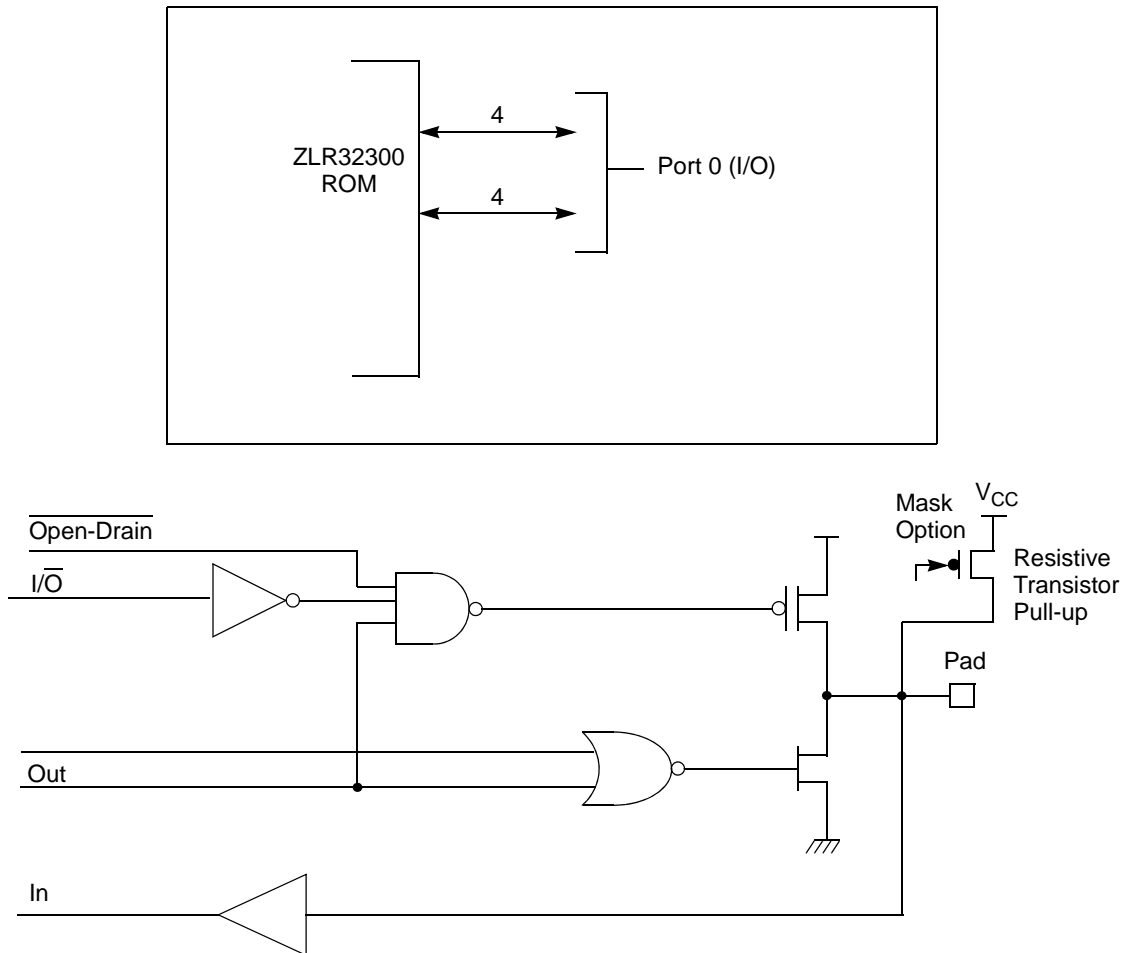


Figure 8. Port 0 Configuration

Port 1 (P17–P10)

Port 1 (see [Figure 9](#)) Port 1 can be configured for standard port input or output mode. After POR, Port 1 is configured as an input port. The output drivers are either push-pull or open-drain and are controlled by bit D1 in the PCON register.

► **Notes:** The Port 1 direction is reset to be input following an SMR.

In 20 and 28-pin packages, Port 1 is reserved. A write to this register will have no effect and will always read FF.

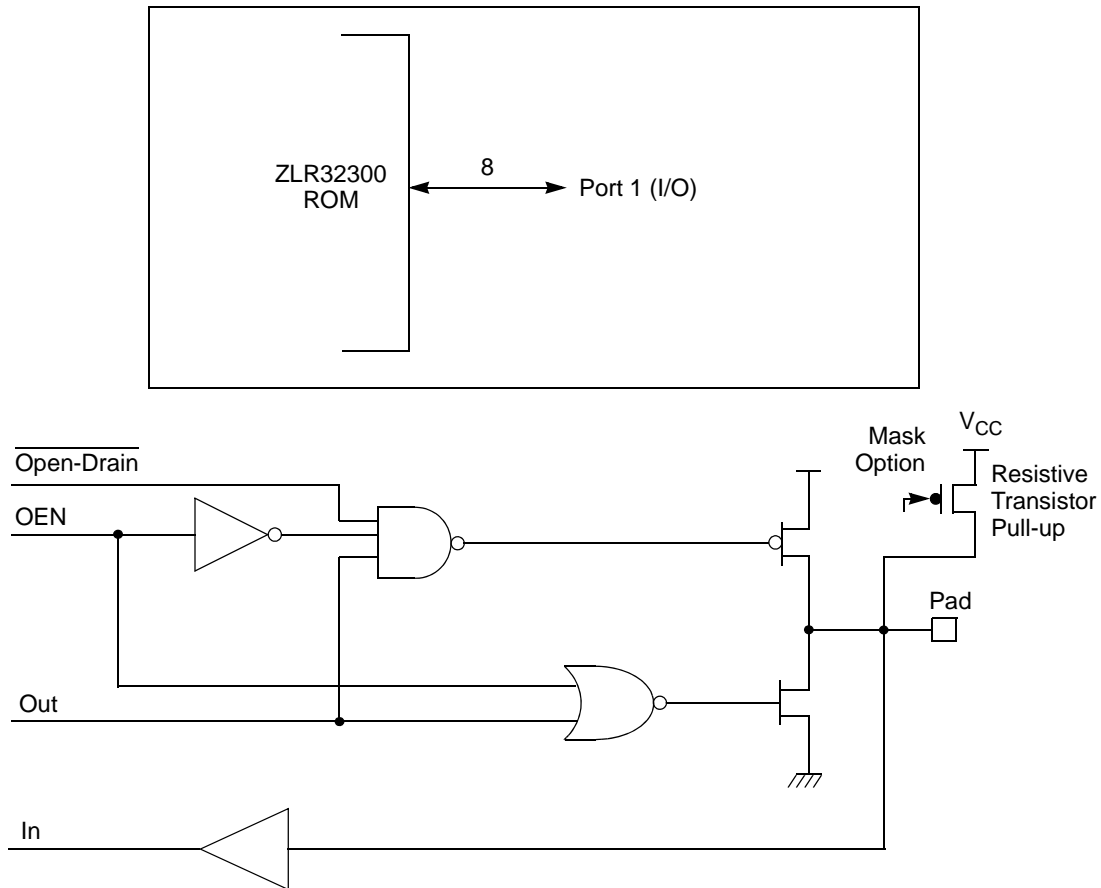


Figure 9. Port 1 Configuration

Port 2 (P27–P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see [Figure 10](#)). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A mask option is available to connect eight pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. The POR resets with the eight bits of Port 2 configured as inputs.

Port 2 also has an 8-bit input OR and AND gate, which can be used to wake up the part. P20 can be programmed to access the edge-detection circuitry in demodulation mode.

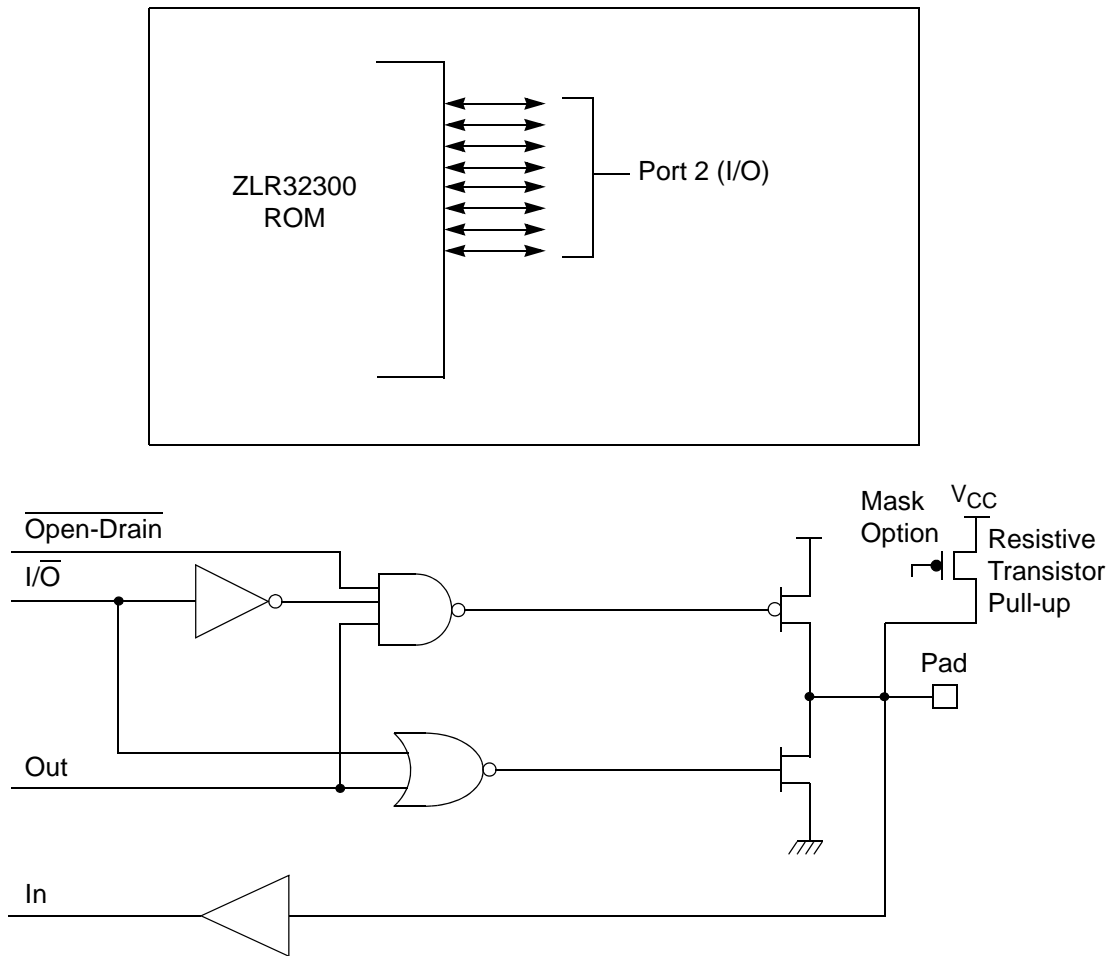


Figure 10. Port 2 Configuration

Port 3 (P37–P30)

Port 3 is a 8-bit, CMOS-compatible fixed I/O port (see [Figure 11](#)). Port 3 consists of four fixed input (P33–P30) and four fixed output (P37–P34), which can be configured under software control for interrupt and as output from the counter/timers. P30, P31, P32, and P33 are standard CMOS inputs; P34, P35, P36, and P37 are push-pull outputs.

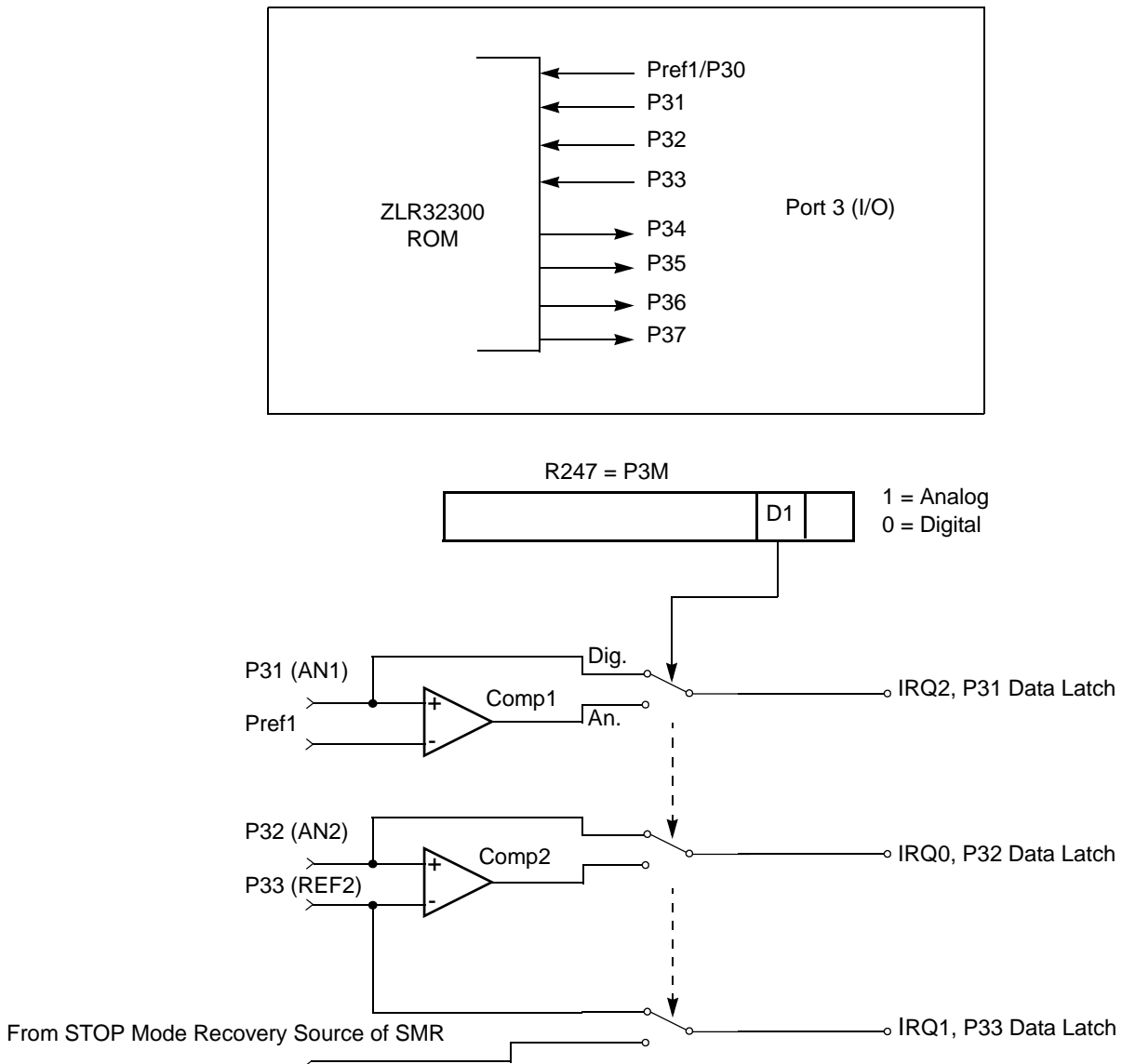


Figure 11. Port 3 Configuration

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edge-

detection circuit is through P31 or P20 (see [T8 and T16 Common Functions—CTR1\(0D\)01h on page 32](#)). Other edge detect and IRQ modes are described in [Table 11](#).

- **Note:** Comparators are powered down by entering STOP mode. For P31–P33 to be used in a STOP Mode Recovery (SMR) source, these inputs must be placed into digital mode.

Table 11. Port 3 Pin Function Summary

Pin	I/O	Counter/Timers	Comparator	Interrupt
Pref1/P30	IN		RF1	
P31	IN	IN	AN1	IRQ2
P32	IN		AN2	IRQ0
P33	IN		RF2	IRQ1
P34	OUT	T8	AO1	
P35	OUT	T16		
P36	OUT	T8/16		
P37	OUT		AO2	
P20	I/O	IN		

Port 3 also provides output for each of the counter/timers and the AND/OR Logic (see [Figure 12](#)). Control is performed by programming bits D5–D4 of CTR1, bit 0 of CTR0, and bit 0 of CTR2.

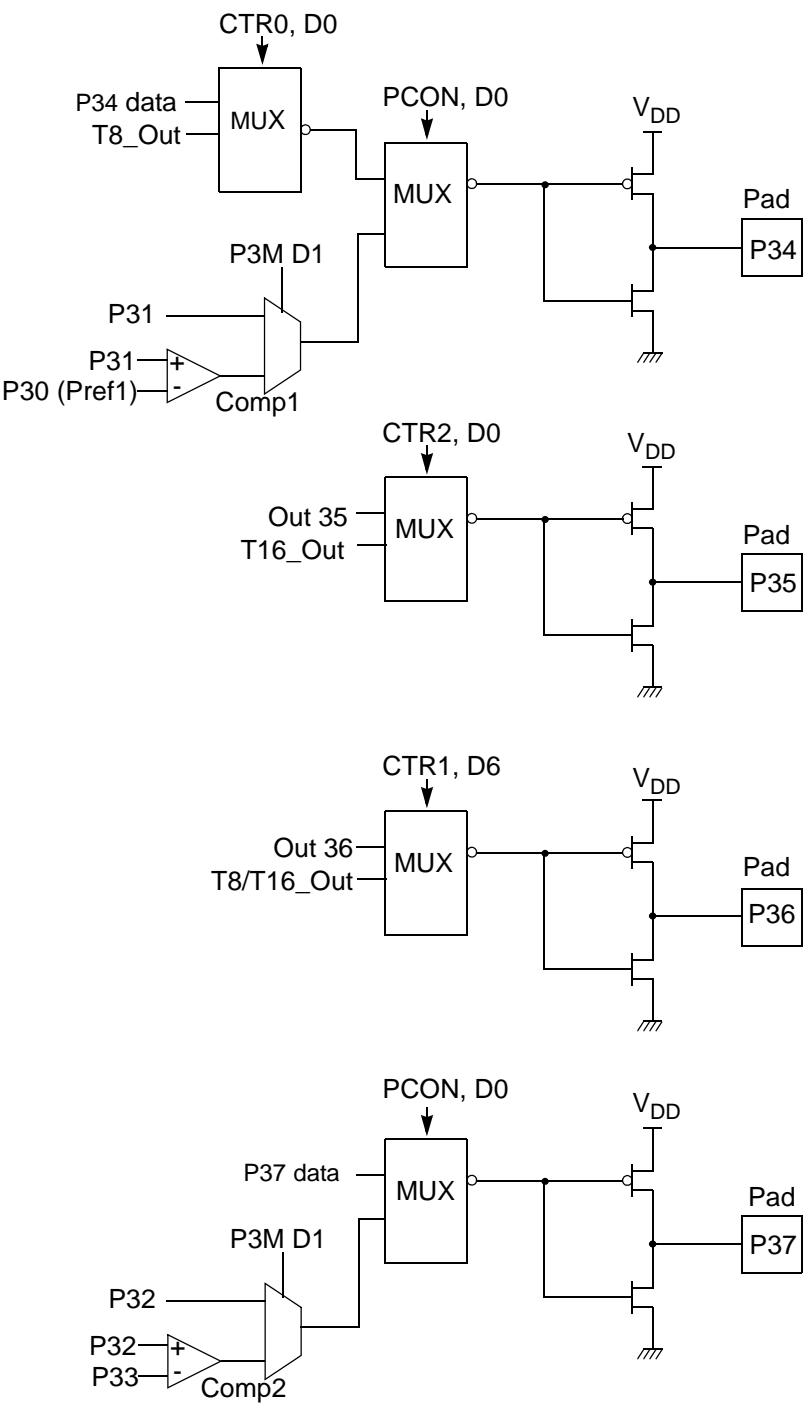


Figure 12. Port 3 Counter/Timer Output Configuration

Comparator Inputs

In analog mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as indicated in [Figure 11](#) on page 19. In digital mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.

- **Note:** Comparators are powered down by entering STOP mode. For P31–P33 to be used in a STOP mode Recovery source, these inputs must be placed into digital mode.

Comparator Outputs

These channels can be programmed to be output on P34 and P37 through the PCON register.

RESET (Input, Active Low)

Reset initializes the MCU and is accomplished either through Power-On, Watch-Dog Timer, STOP mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the external reset line must be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally.

When the ZLR32300 asserts (Low) the RESET pin, the internal pull-up is disabled. The ZLR32300 does not assert the RESET pin when under VBO.

- **Note:** The external Reset does not initiate an exit from STOP mode.

Functional Description

This device incorporates special functions to enhance the Z8[®] functionality in consumer and battery-operated applications.

Program Memory

This device addresses 32KB of ROM memory. The first 12 Bytes are reserved for interrupt vectors. These locations contain the six 16-bit vectors that correspond to the six available interrupts. See [Figure 13](#).

RAM

This device features 256B of RAM.

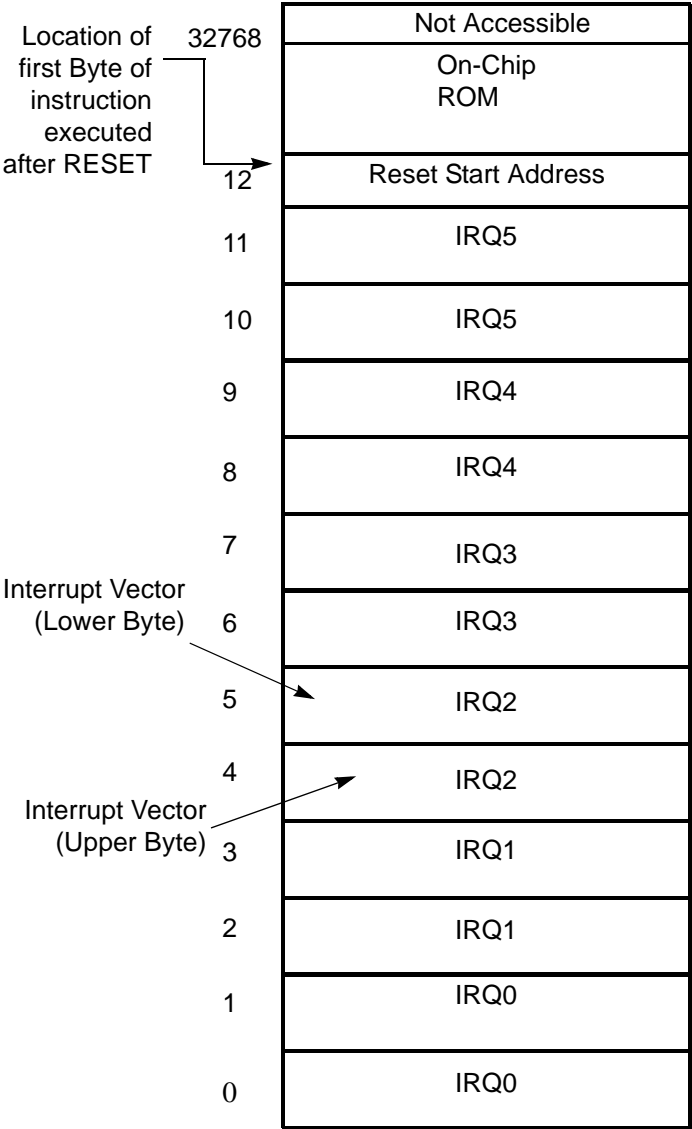


Figure 13. Program Memory Map (32K ROM)

Expanded Register File

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The Z8® register address space (R0 through R15) has been implemented as 16 banks, with 16 registers per bank. These register groups are known as the



ERF (Expanded Register File). Bits 7–4 of register RP select the working register group. Bits 3–0 of register RP select the expanded register file bank.

- **Note:** An expanded register bank is also referred to as an expanded register group (see [Figure 14](#)).

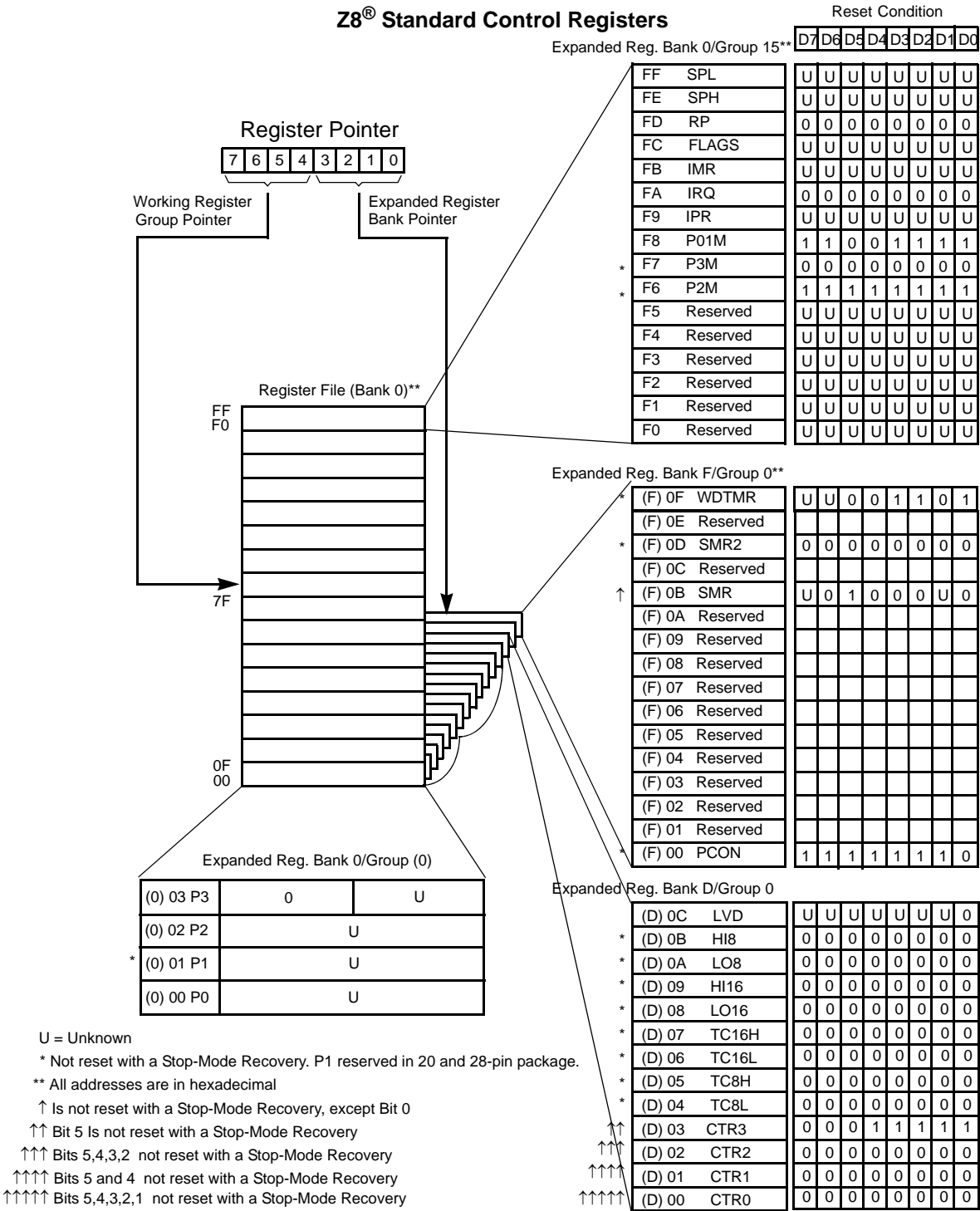


Figure 14. Expanded Register File Architecture

The upper nibble of the register pointer (see [Figure 15](#)) selects which working register group, of 16 bytes in the register file, is accessed out of the possible 256. The lower nibble selects the expanded register file bank and, in the case of the Crimzon™ ZLR32300 family, banks 0, F, and D are implemented. A 0h in the lower nibble allows the normal register file (bank 0) to be addressed. Any other value from 1h to Fh exchanges the lower 16 registers to an expanded register bank.

R253 RP

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

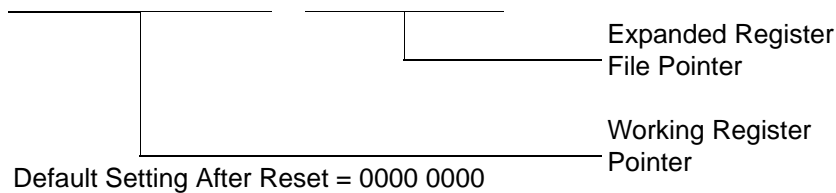


Figure 15. Register Pointer

Example: Crimzon™ ZLR32300: (See [Figure 14](#) on page 25)

R253 RP = 00h

R0 = Port 0

R1 = Port 1

R2 = Port 2

R3 = Port 3

But if:

R253 RP = 0Dh

R0 = CTR0

R1 = CTR1

R2 = CTR2

R3 = CTR3

The counter/timers are mapped into ERF group D. Access is easily performed using the following:

```

LD          RP, #0Dh          ; Select ERF D
for access to bank D

                                ; (working
                                ; register group 0)
LD          R0, #xx           ; load CTR0
LD          1, #xx            ; load CTR1
LD          R1, 2              ; CTR2→CTR1

LD          RP, #0Dh          ; Select ERF D
for access to bank D

                                ; (working
                                ; register group 0)
LD          RP, #7Dh          ; Select
expanded register bank D and working ; register
group 7 of bank 0 for access.
LD          71h, 2
; CTR2→register 71h
LD          R1, 2
; CTR2→register 71h

```

Register File

The register file (bank 0) consists of 4 I/O port registers, 237 general-purpose registers, 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), and two expanded registers groups in Banks D (see [Table 12](#)) and F. Instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing a short, 4-bit register address to use the Register Pointer ([Figure 16](#)). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

- **Note:** Working register group E0–EF can only be accessed through working registers and indirect addressing modes.

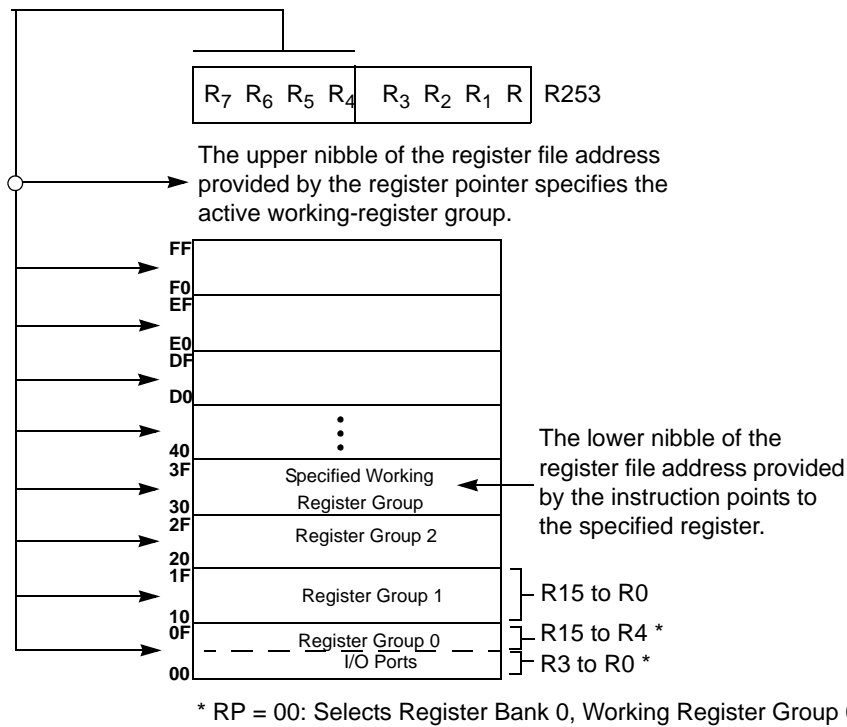


Figure 16. Register Pointer—Detail

Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.

Timers

T8_Capture_HI—HI8(D)0BH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 1.

Field	Bit Position		Description
T8_Capture_HI	[7:0]	R/W	Captured Data - No Effect

T8_Capture_LO—L08(D)0AH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 0.

Field	Bit Position		Description
T8_Capture_LO	[7:0]	R/W	Captured Data - No Effect

T16_Capture_HI—HI16(D)09H

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

Field	Bit Position		Description
T16_Capture_HI	[7:0]	R/W	Captured Data - No Effect

T16_Capture_LO—L016(D)08H

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

Field	Bit Position		Description
T16_Capture_LO	[7:0]	R/W	Captured Data - No Effect

Counter/Timer2 MS-Byte Hold Register—TC16H(D)07H

Field	Bit Position		Description
T16_Data_HI	[7:0]	R/W	Data

Counter/Timer2 LS-Byte Hold Register—TC16L(D)06H

Field	Bit Position	Description
T16_Data_LO	[7:0]	R/W Data

Counter/Timer8 High Hold Register—TC8H(D)05H

Field	Bit Position	Description
T8_Level_HI	[7:0]	R/W Data

Counter/Timer8 Low Hold Register—TC8L(D)04H

Field	Bit Position	Description
T8_Level_LO	[7:0]	R/W Data

CTR0 Counter/Timer8 Control Register—CTR0(D)00H

Table 12 lists and briefly describes the fields for this register.

Table 12. CTR0(D)00H Counter/Timer8 Control Register

Field	Bit Position		Value	Description
T8_Enable	7-----	R/W	0*	Counter Disabled
			1	Counter Enabled
			0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6-----	R/W	0*	Modulo-N
			1	Single Pass
Time_Out	--5-----	R/W	0**	No Counter Time-Out
			1	Counter Time-Out Occurred
			0	No Effect
			1	Reset Flag to 0
T8_Clock	---43---	R/W	0 0**	SCLK
			0 1	SCLK/2
			1 0	SCLK/4
			1 1	SCLK/8
Capture_INT_Mask	-----2--	R/W	0**	Disable Data Capture Interrupt
			1	Enable Data Capture Interrupt

Table 12. CTR0(D)00H Counter/Timer8 Control Register (Continued)

Field	Bit Position		Value	Description
Counter_INT_Mask	-----1-	R/W	0**	Disable Time-Out Interrupt
			1	Enable Time-Out Interrupt
P34_Out	-----0	R/W	0*	P34 as Port Output
			1	T8 Output on P34

Note:

*Indicates the value upon Power-On Reset.

**Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

T8 Enable

This field enables T8 when set (written) to 1.

Single/Modulo-N

When set to 0 (Modulo-N), the counter reloads the initial value when the terminal count is reached. When set to 1 (single-pass), the counter stops when the terminal count is reached.

Timeout

This bit is set when T8 times out (terminal count reached). To reset this bit, write a 1 to its location.



Caution: Writing a 1 is the only way to reset the Terminal Count status condition. Reset this bit before using/enabling the counter/timers.

The first clock of T8 might not have complete clock width and can occur any time when enabled.



Note: Take care when using the OR or AND commands to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (Demodulation Mode). These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers is ORed or ANDed with the designated value and then written back into the registers.

T8 Clock

These bits define the frequency of the input signal to T8.

Capture_INT_Mask

Set this bit to allow an interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in demodulation mode.

Counter_INT_Mask

Set this bit to allow an interrupt when T8 has a timeout.

P34_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

T8 and T16 Common Functions—CTR1(0D)01h

This register controls the functions in common with the T8 and T16.

[Table 13](#) lists and briefly describes the fields for this register.

Table 13. CTR1(0D)01H T8 and T16 Common Functions

Field	Bit Position		Value	Description
Mode	7-----	R/W	0*	Transmit Mode
			1	Demodulation Mode
P36_Out/ Demodulator_Input	-6-----	R/W	0*	Transmit Mode
			1	Port Output
			0*	T8/T16 Output
			1	Demodulation Mode
T8/T16_Logic/ Edge_Detect	--54----	R/W	00**	P31
			01	P20
			10	Transmit Mode
			11	AND
			00**	OR
			01	NOR
			10	NAND
			11	Demodulation Mode
			00**	Falling Edge
			01	Rising Edge
			10	Both Edges
			11	Reserved

Table 13. CTR1(0D)01H T8 and T16 Common Functions (Continued)

Field	Bit Position		Value	Description
Transmit_Submode/ Glitch_Filter	----32--	R/W	00	Transmit Mode
			01	Normal Operation
			10	Ping-Pong Mode
			11	T16_Out = 0
			11	T16_Out = 1
			00	Demodulation Mode
			01	No Filter
			10	4 SCLK Cycle
			11	8 SCLK Cycle
			11	Reserved
Initial_T8_Out/ Rising Edge	-----1-	R/W	0	Transmit Mode
			1	T8_OUT is 0 Initially
		R	0	T8_OUT is 1 Initially
			1	Demodulation Mode
		W	0	No Rising Edge
			1	Rising Edge Detected
			0	No Effect
			1	Reset Flag to 0
Initial_T16_Out/ Falling_Edge	-----0	R/W	0	Transmit Mode
			1	T16_OUT is 0 Initially
		R	0	T16_OUT is 1 Initially
			1	Demodulation Mode
		W	0	No Falling Edge
			1	Falling Edge Detected
			0	No Effect
			1	Reset Flag to 0

Note:

*Default at Power-On Reset.

**Default at Power-On Reset. Not reset with a Stop Mode recovery.

Mode

If the result is 0, the counter/timers are in TRANSMIT mode; otherwise, they are in DEMODULATION mode.

P36_Out/Demodulator_Input

In TRANSMIT Mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In DEMODULATION Mode, this bit defines whether the input signal to the Counter/Timers is from P20 or P31.

If the input signal is from Port 31, a capture event may also generate an IRQ2 interrupt. To prevent generating an IRQ2, either disable the IRQ2 interrupt by clearing its IMR bit D2 or use P20 as the input.

T8/T16_Logic/Edge _Detect

In TRANSMIT Mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In DEMODULATION Mode, this field defines which edge should be detected by the edge detector.

Transmit_Submode/Glitch Filter

In Transmit Mode, this field defines whether T8 and T16 are in the PING-PONG mode or in independent normal operation mode. Setting this field to “NORMAL OPERATION Mode” terminates the “PING-PONG Mode” operation. When set to 10, T16 is immediately forced to a 0; a setting of 11 forces T16 to output a 1.

In DEMODULATION Mode, this field defines the width of the glitch that must be filtered out.

Initial_T8_Out/Rising_Edge

In TRANSMIT Mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When the counter is not enabled and this bit is set to 1 or 0, T8_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D1.

In DEMODULATION Mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset the mode, a 1 should be written to this location.

Initial_T16 Out/Falling _Edge

In TRANSMIT Mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or PING-PONG Mode (CTR1, D3; D2). When the counter is not enabled and this bit is set, T16_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D0.

In DEMODULATION Mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

- **Note:** Modifying CTR1 (D1 or D0) while the counters are enabled causes unpredictable output from T8/T16_OUT.

CTR2 Counter/Timer 16 Control Register—CTR2(D)02H

Table 14 lists and briefly describes the fields for this register.

Table 14. CTR2(D)02H: Counter/Timer16 Control Register

Field	Bit Position		Value	Description
T16_Enable	7-----	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6-----	R/W	0*	Transmit Mode
			1	Modulo-N
			0	Single Pass
			1	Demodulation Mode
Time_Out	--5-----	R	0**	T16 Recognizes Edge
			1	T16 Does Not Recognize Edge
		W	0	No Counter Timeout
			1	Counter Timeout Occurred
T16_Clock	---43---	R/W	00**	No Effect
			01	Reset Flag to 0
			10	SCLK
			11	SCLK/2
Capture_INT_Mask	-----2--	R/W	0**	SCLK/4
			1	SCLK/8
Counter_INT_Mask	-----1-	R/W	0*	Disable Data Capture Int.
			1	Enable Data Capture Int.
P35_Out	-----0	R/W	0*	Disable Timeout Int.
			1	Enable Timeout Int.

Note:

*Indicates the value upon Power-On Reset.

**Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

T16_Enable

This field enables T16 when set to 1.

Single/Modulo-N

In TRANSMIT Mode, when set to 0, the counter reloads the initial value when it reaches the terminal count. When set to 1, the counter stops when the terminal count is reached.

In DEMODULATION Mode, when set to 0, T16 captures and reloads on detection of all the edges. When set to 1, T16 captures and detects on the first edge but ignores the subsequent edges. For details, see the description of T16 Demodulation Mode on page 44.

Time_Out

This bit is set when T16 times out (terminal count reached). To reset the bit, write a 1 to this location.

T16_Clock

This bit defines the frequency of the input signal to Counter/Timer16.

Capture_INT_Mask

This bit is set to allow an interrupt when data is captured into LO16 and HI16.

Counter_INT_Mask

Set this bit to allow an interrupt when T16 times out.

P35_Out

This bit defines whether P35 is used as a normal output pin or T16 output.

CTR3 T8/T16 Control Register—CTR3(D)03H

[Table 15](#) lists and briefly describes the fields for this register. This register allows the T₈ and T₁₆ counters to be synchronized.

Table 15. CTR3 (D)03H: T8/T16 Control Register

Field	Bit Position		Value	Description
T ₁₆ Enable	7-----	R	0**	Counter Disabled
		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
T ₈ Enable	-6-----	R	0**	Counter Disabled
		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
Sync Mode	--5-----	R/W	0*	Disable Sync Mode
			1	Enable Sync Mode

Table 15. CTR3 (D)03H: T8/T16 Control Register (Continued)

Field	Bit Position		Value	Description
Reserved	---43210	R	1	Always reads 11111
		W	x	No Effect

Note: *Indicates the value upon Power-On Reset.

**Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

Counter/Timer Functional Blocks

Input Circuit

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5–D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal that have a width less than specified (CTR1 D3, D2) are filtered out (see [Figure 17](#)).

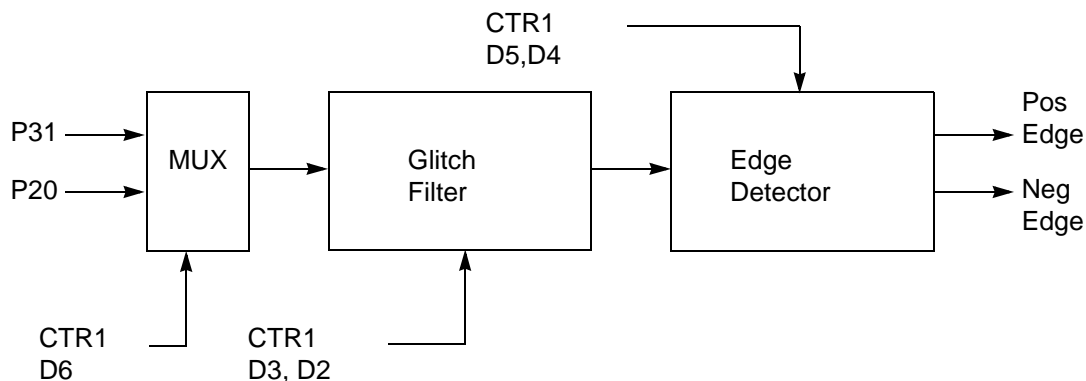


Figure 17. Glitch Filter Circuitry

T8 Transmit Mode

Before T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8_OUT is 1; if it is 1, T8_OUT is 0. See [Figure 18](#).

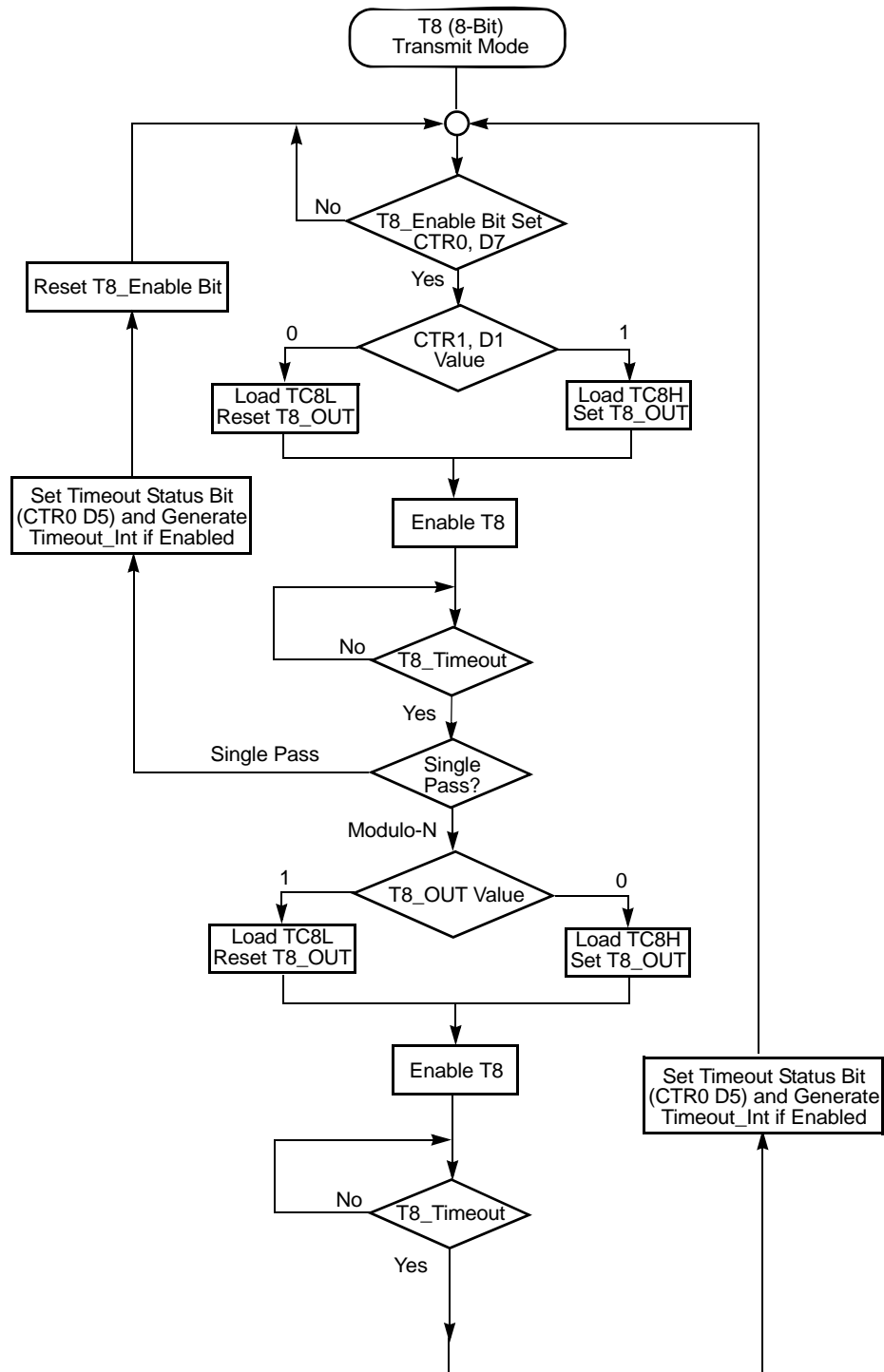


Figure 18. Transmit Mode Flowchart

When T8 is enabled, the output T8_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In SINGLE-PASS Mode (CTR0, D6), T8 counts down to 0 and stops, T8_OUT toggles, the timeout status bit (CTR0, D5) is set, and a timeout interrupt can be generated if it is enabled (CTR0, D1). In Modulo-N Mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, and sets the timeout status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8_OUT level and repeats the cycle. See [Figure 19](#).

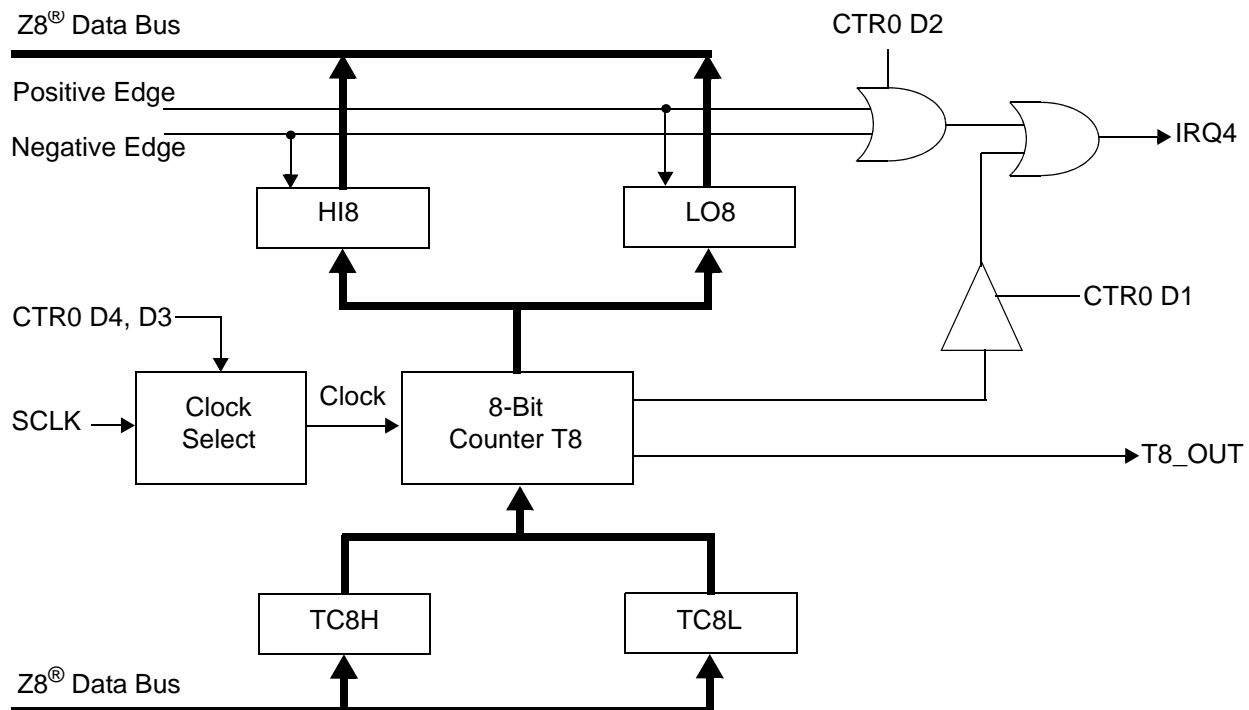


Figure 19. 8-Bit Counter/Timer Circuits

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.



Caution: To ensure known operation do not write these registers at the time the values are to be loaded into the counter/timer.

An initial count of 1 is not allowed (a non-function occurs). An initial count of 0 causes TC8 to count from 0 to FFH to FEH.

► **Note:** The letter H denotes hexadecimal values.

Transition from 0 to FFH is not a timeout condition.



Caution: Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur. See [Figure 20](#) and [Figure 21](#).

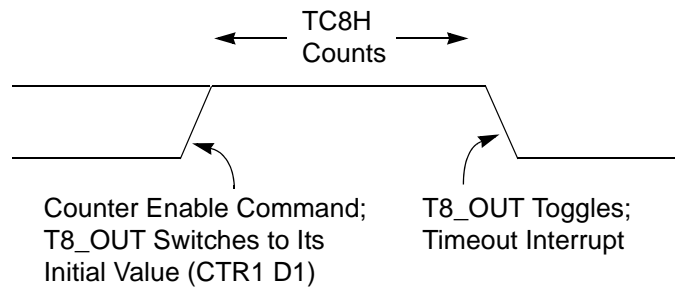


Figure 20. T8_OUT in Single-Pass Mode

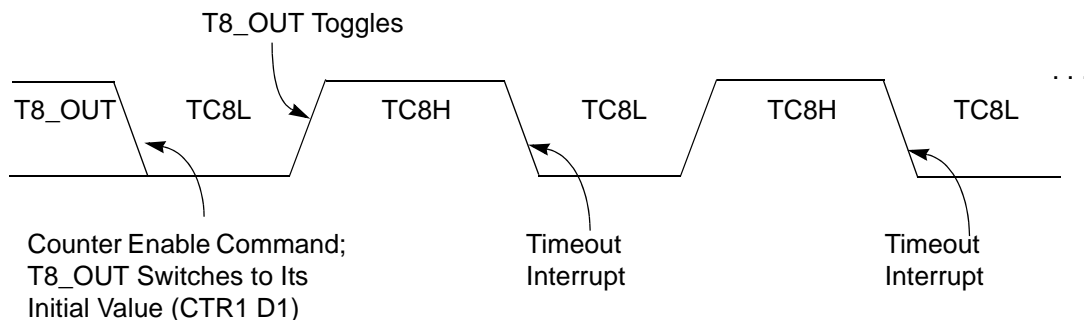


Figure 21. T8_OUT in Modulo-N Mode

T8 Demodulation Mode

The user must program TC8L and TC8H to FFh. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to

count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the timeout status bit (CTR0, D5) is set, and an interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from FFh (see Figure 22 and Figure 23).

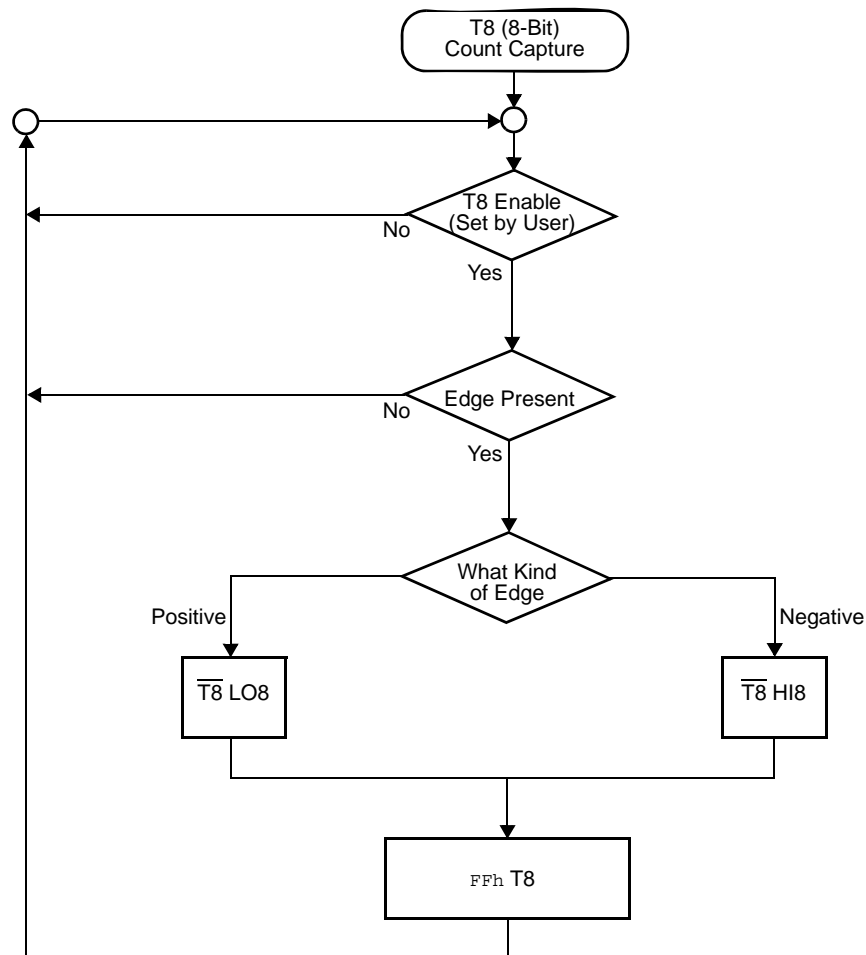


Figure 22. Demodulation Mode Count Capture Flowchart

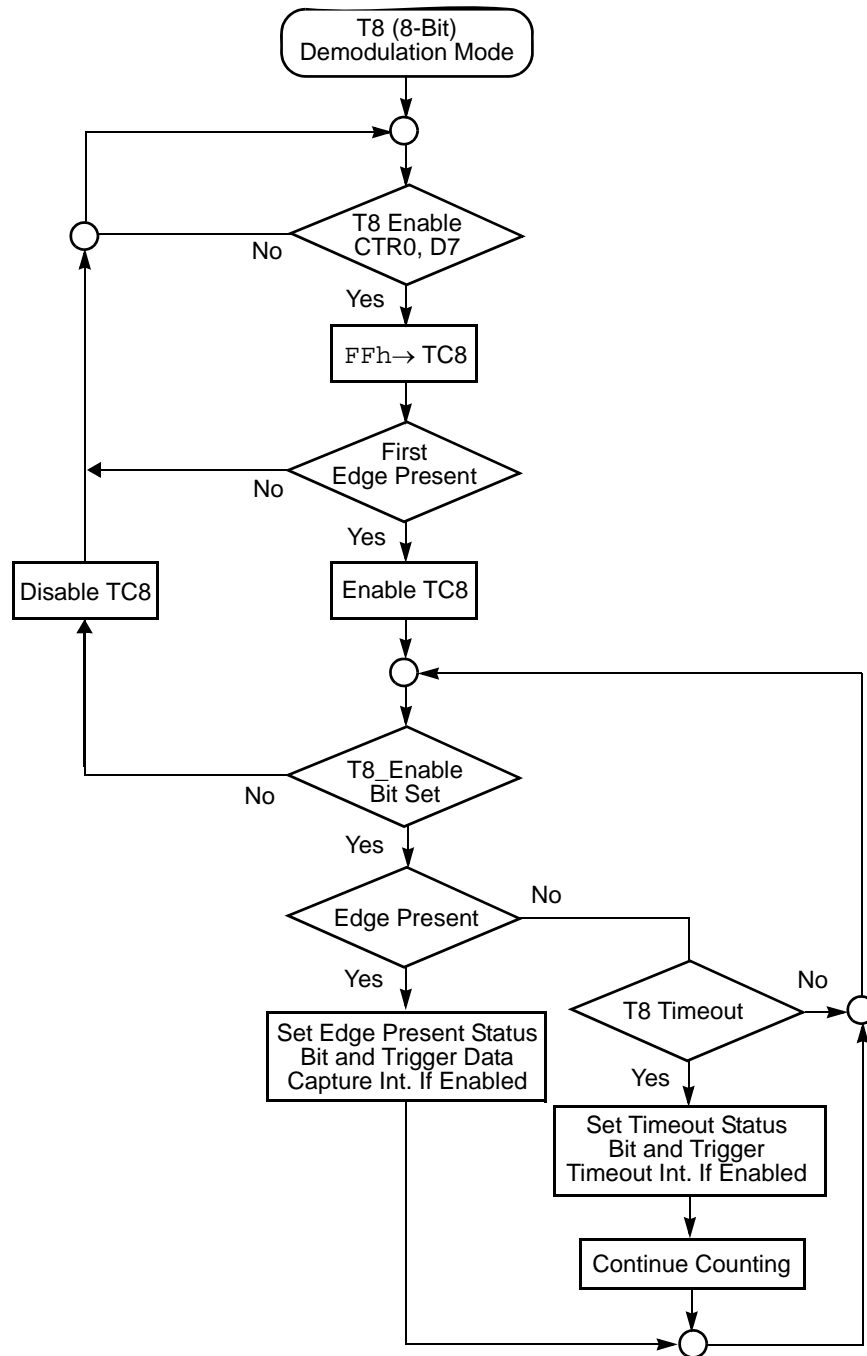


Figure 23. Demodulation Mode Flowchart

T16 Transmit Mode

In NORMAL or PING-PONG mode, the output of T16 when not enabled, is dependent on CTR1, D0. If it is a 0, T16_OUT is a 1; if it is a 1, T16_OUT is 0. You can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3; D2 to a 10 or 11.

When T16 is enabled, TC16H * 256 + TC16L is loaded, and T16_OUT is switched to its initial value (CTR1, D0). When T16 counts down to 0, T16_OUT is toggled (in NORMAL or PING-PONG mode), an interrupt (CTR2, D1) is generated (if enabled), and a status bit (CTR2, D5) is set. See [Figure 24](#).

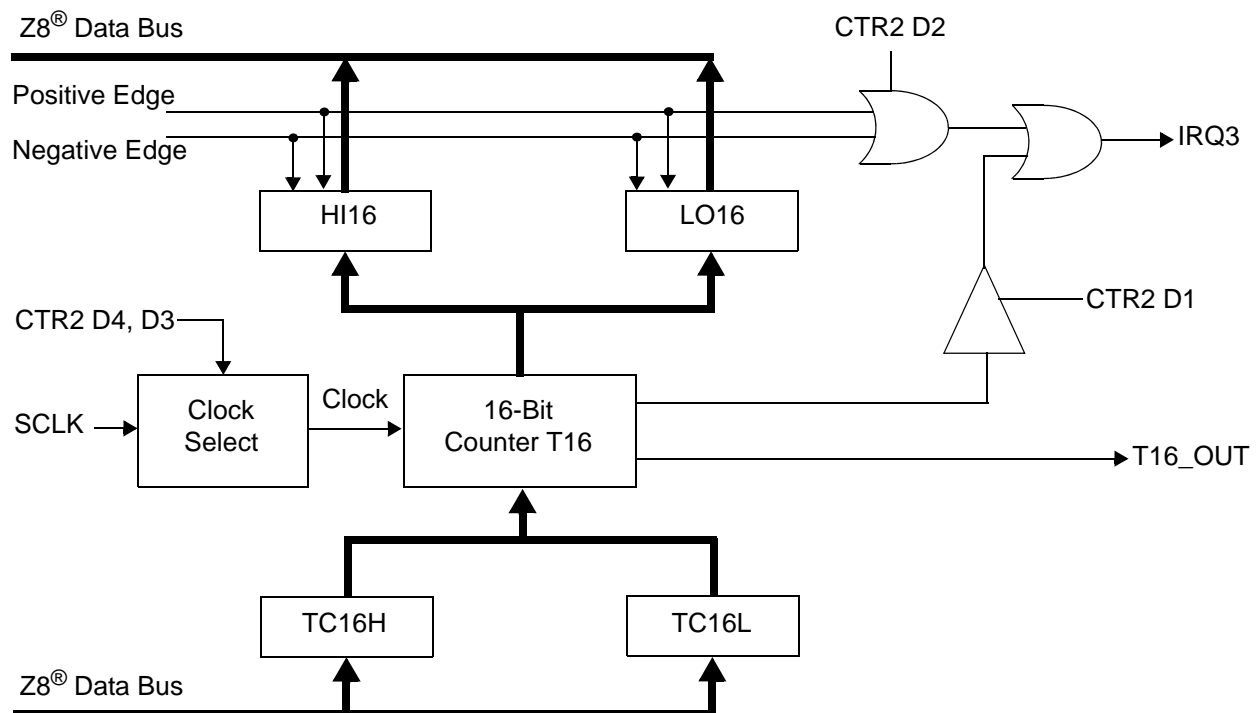


Figure 24. 16-Bit Counter/Timer Circuits

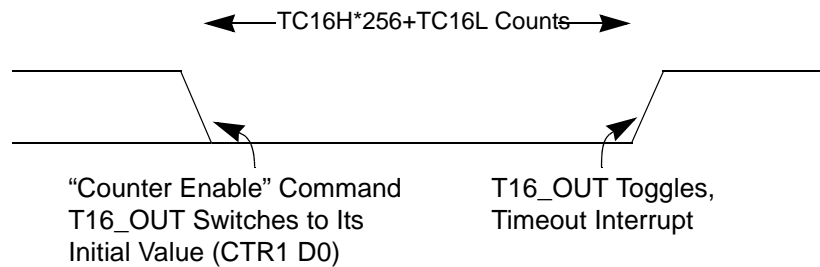
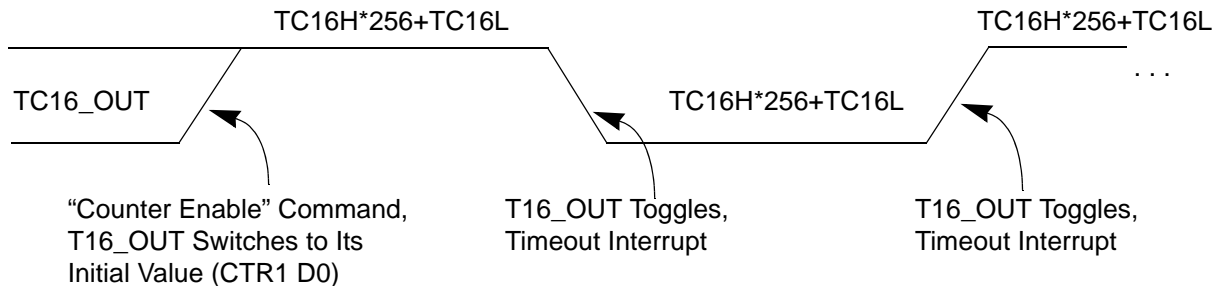
► **Note:** Global interrupts override this function as described in [Interrupts on page 47](#).

If T16 is in SINGLE-PASS mode, it is stopped at this point (see [Figure 25](#)). If it is in Modulo-N Mode, it is loaded with $TC16H * 256 + TC16L$, and the counting continues (see [Figure 26](#)).

You can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded.

**Caution:**

Do not load these registers at the time the values are to be loaded into the counter/timer to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to FFFFH to FFFE_H. Transition from 0 to FFFF_H is not a timeout condition.

**Figure 25. T16_OUT in Single-Pass Mode****Figure 26. T16_OUT in Modulo-N Mode****T16 DEMODULATION Mode**

The user must program TC16L and TC16H to FF_H. After T16 is enabled, and the first edge (rising, falling, or both depending on CTR1 D5; D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

If D6 of CTR2 Is 0

When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current count in T16 is complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt is generated if enabled (CTR2, D2). T16 is loaded with FFFF_H and starts again.

This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).

If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A timeout of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both depending on CTR1, D5; D4), continuing to ignore subsequent edges.

This T16 mode generally measures mark time, the length of an active carrier signal burst.

If T16 reaches 0, T16 continues counting from `FFFFH`. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt timeout can be generated if enabled (CTR2 D1).

Ping-Pong Mode

This operation mode is only valid in TRANSMIT Mode. T8 and T16 must be programmed in Single-Pass mode (CTR0, D6; CTR2, D6), and Ping-Pong mode must be programmed in CTR1, D3; D2. The user can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR2, D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1, D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the ping-pong operation, write 00 to bits D3 and D2 of CTR1. See [Figure 27](#).

- **Note:** Enabling ping-pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and reset the status flags before instituting this operation.

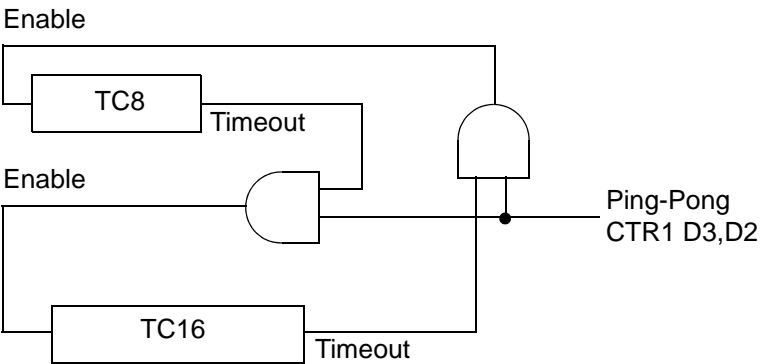


Figure 27. Ping-Pong Mode Diagram

Initiating PING-PONG Mode

First, make sure both counter/timers are not running. Set T8 into Single-Pass mode (CTR0, D6), set T16 into SINGLE-PASS mode (CTR2, D6), and set the Ping-Pong mode (CTR1, D2; D3). These instructions can be in random order. Finally, start PING-PONG mode by enabling either T8 (CTR0, D7) or T16 (CTR2, D7). See [Figure 28](#).

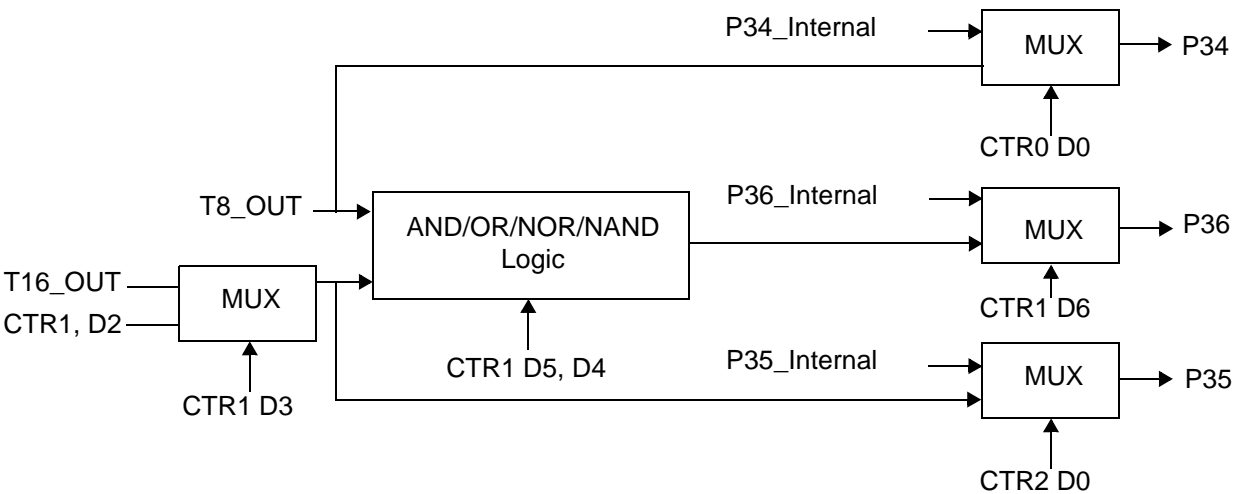


Figure 28. Output Circuit

The initial value of T8 or T16 must not be 1. If you stop the timer and restart the timer, reload the initial value to avoid an unknown previous value.

During PING-PONG Mode

The enable bits of T8 and T16 (CTR0, D7; CTR2, D7) are set and cleared alternately by hardware. The timeout bits (CTR0, D5; CTR2, D5) are set every time the counter/timers reach the terminal count.

Timer Output

The output logic for the timers is illustrated in [Figure 28](#). P34 is used to output T8-OUT when D0 of CTR0 is set. P35 is used to output the value of T16-OUT when D0 of CTR2 is set. When D6 of CTR1 is set, P36 outputs the logic combination of T8-OUT and T16-OUT determined by D5 and D4 of CTR1.

Interrupts

The Crimzon™ ZLR32300 features six different interrupts ([Table 16](#)). The interrupts are maskable and prioritized ([Figure 29](#)). The six sources are divided as follows: three sources are claimed by Port 3 lines P33–P31, two by the counter/timers ([Table 16](#)) and one for low voltage detection. The Interrupt Mask Register (globally or individually) enables or disables the six interrupt requests.

The source for IRQ is determined by bit 1 of the Port 3 mode register (P3M). When in digital mode, Pin P33 is the source. When in analog mode the output of the stop mode recovery source logic is used as the source for the interrupt. See [Figure 34](#).

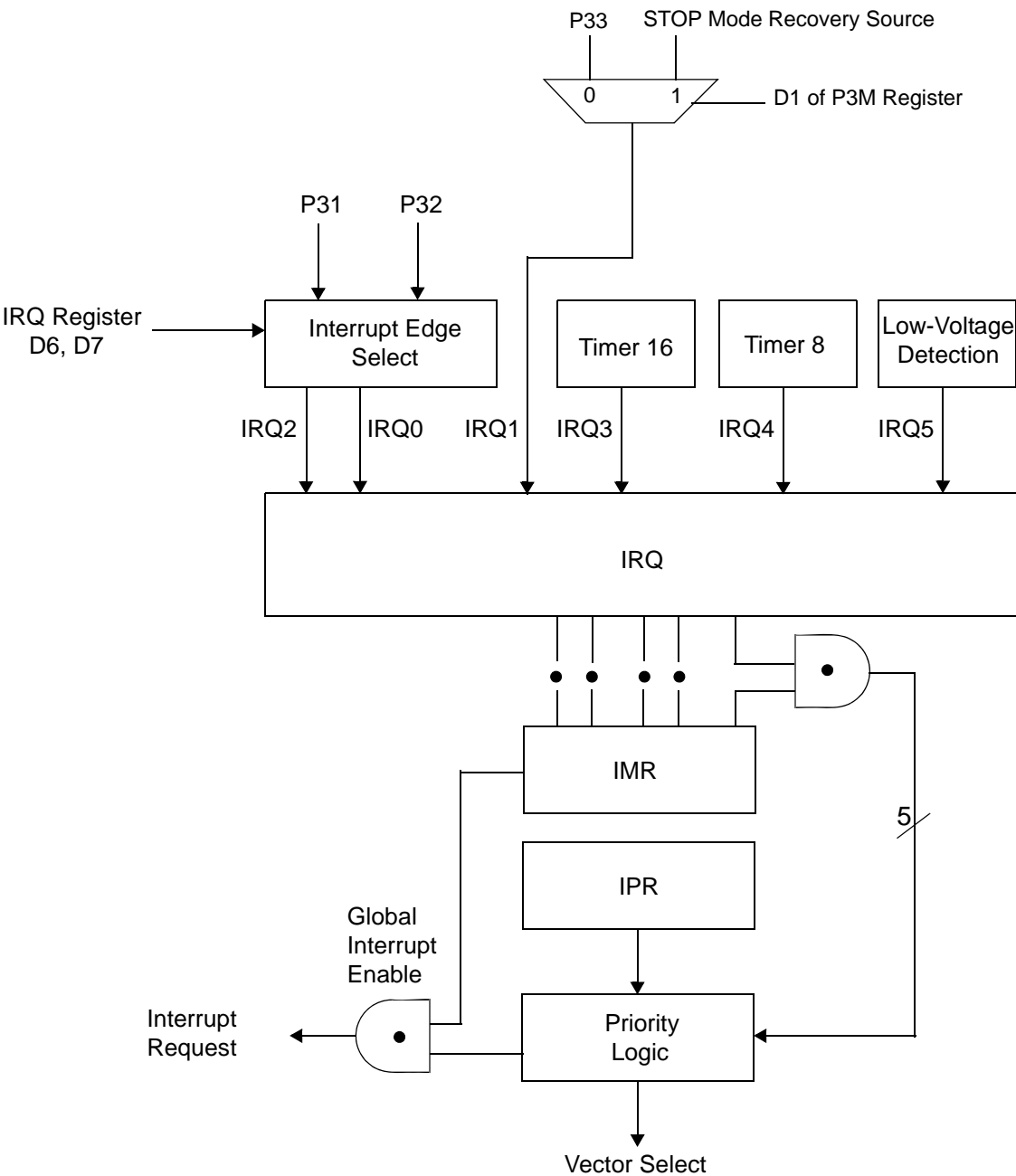


Figure 29. Interrupt Block Diagram

Table 16. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	P32	0,1	External (P32), Rising, Falling Edge Triggered
IRQ1	P33	2,3	External (P33), Falling Edge Triggered
IRQ2	P31, T _{IN}	4,5	External (P31), Rising, Falling Edge Triggered
IRQ3	T16	6,7	Internal
IRQ4	T8	8,9	Internal
IRQ5	LVD	10,11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority Register. An interrupt machine cycle activates when an interrupt request is granted. As a result, all subsequent interrupts are disabled, and the Program Counter and Status Flags are saved. The cycle then branches to the program memory vector location reserved for that interrupt. All Crimzon™ ZLR32300 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked, and the Interrupt Request register is polled to determine which of the interrupt requests require service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 can be rising, falling, or both edge triggered. These interrupts are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is indicated in [Table 17](#).

Table 17. IRQ Register

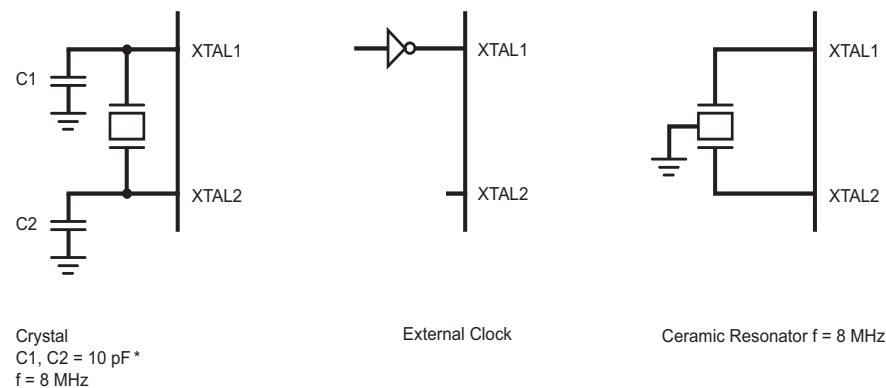
IRQ		Interrupt Edge	
D7	D6	IRQ2 (P31)	IRQ0 (P32)
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Note: F = Falling Edge; R = Rising Edge

Clock

The device's on-chip oscillator has a high-gain, parallel-resonant amplifier, for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal must be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100 Ω . The on-chip oscillator can be driven with a suitable external clock source.

The crystal must be connected across XTAL1 and XTAL2 using the recommended capacitors from each pin to ground. The typical capacitor value is 10pF for 8MHz. Also check with the crystal supplier for the optimum capacitance.



*Note: preliminary value.

Figure 30. Oscillator Configuration

ZiLOG IR MCU supports crystal, resonator, and oscillator. Most resonators have a frequency tolerance of less than $\pm 0.5\%$, which is enough for remote control application. Resonator has a very fast startup time, which is around few hundred microseconds. Most crystals have a frequency tolerance of less than 50 ppm ($\pm 0.005\%$). However, crystal needs longer startup time than the resonator. The large loading capacitance slows down the oscillation startup time. ZiLOG suggests not to use more than 10pF loading capacitor for the crystal. If the stray capacitance of the PCB or the crystal is high, the loading capacitance C1 and C2 must be reduced further to ensure stable oscillation before the T_{POR} (Power-On Reset time is typically 5-6 ms. Refer to [AC Characteristics in Table 10](#)).

For Stop Mode Recovery operation, bit 5 of SMR register allows you to select the STOP mode recovery delay, which is the T_{POR} . If STOP mode recovery delay is not selected, the MCU executes instruction immediately after it wakes up from the

STOP mode. If resonator or crystal is used as a clock source then STOP mode recovery delay needs to be selected (bit 5 of SMR = 1).

For both resonator and crystal oscillator, the oscillation ground must go directly to the ground pin of the microcontroller. The oscillation ground must use the shortest distance from the microcontroller ground pin and it must be isolated from other connections.

Power Management

Power-On Reset

A timer circuit clocked by a dedicated on-board RC-oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{DD} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK status, including Waking up from V_{BO} Standby
- Stop-Mode Recovery (if D5 of SMR = 1)
- WDT Timeout

The POR timer is 2.5 ms minimum. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock).

HALT Mode

This instruction turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, IRQ4, and IRQ5 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after HALT Mode.

STOP Mode

This instruction turns off the internal clock and external crystal oscillation, reducing the standby current to 10 μ A or less. STOP Mode is terminated only by a reset, such as WDT timeout, POR, SMR or external reset. This condition causes the processor to restart the application program at address 000CH. To enter STOP (or HALT) mode, first flush the instruction pipeline to avoid suspending execution in mid-instruction. Execute a NOP (Opcode = FFH) immediately before the appropriate sleep instruction, as follows:

```

FF      NOP      ; clear the pipeline
6F      STOP     ; enter STOP mode

or

FF      NOP      ; clear the pipeline
7F      HALT     ; enter HALT Mode

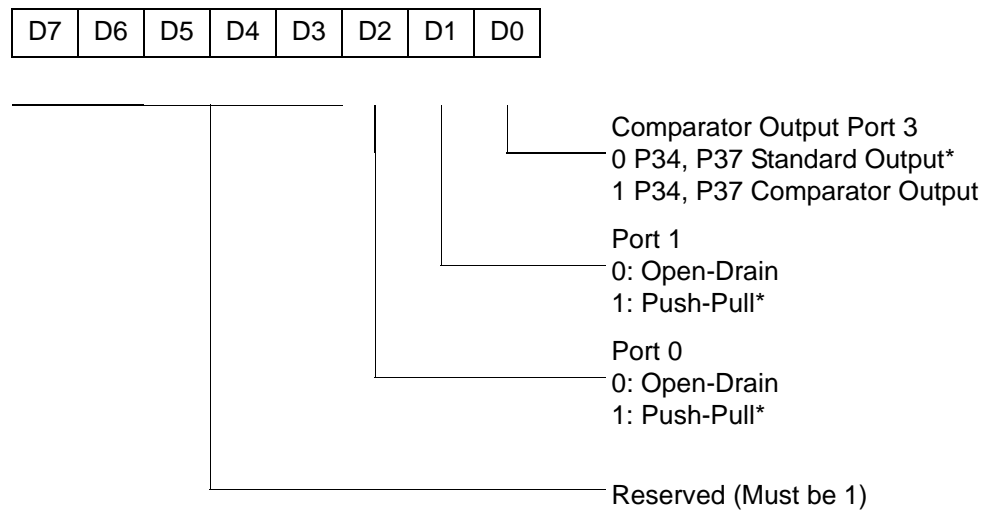
```

Port Configuration

Port Configuration Register

The Port Configuration (PCON) register ([Figure 31](#)) configures the comparator output on Port 3. It is located in the expanded register 2 at Bank F, location 00.

PCON(FH)00h



* Default setting after reset

Figure 31. Port Configuration Register (PCON) (Write Only)

Comparator Output Port 3 (D0)

Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration.

Port 1 Output Mode (D1)

Bit 1 controls the output mode of port 1. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

Port 0 Output Mode (D2)

Bit 2 controls the output mode of port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

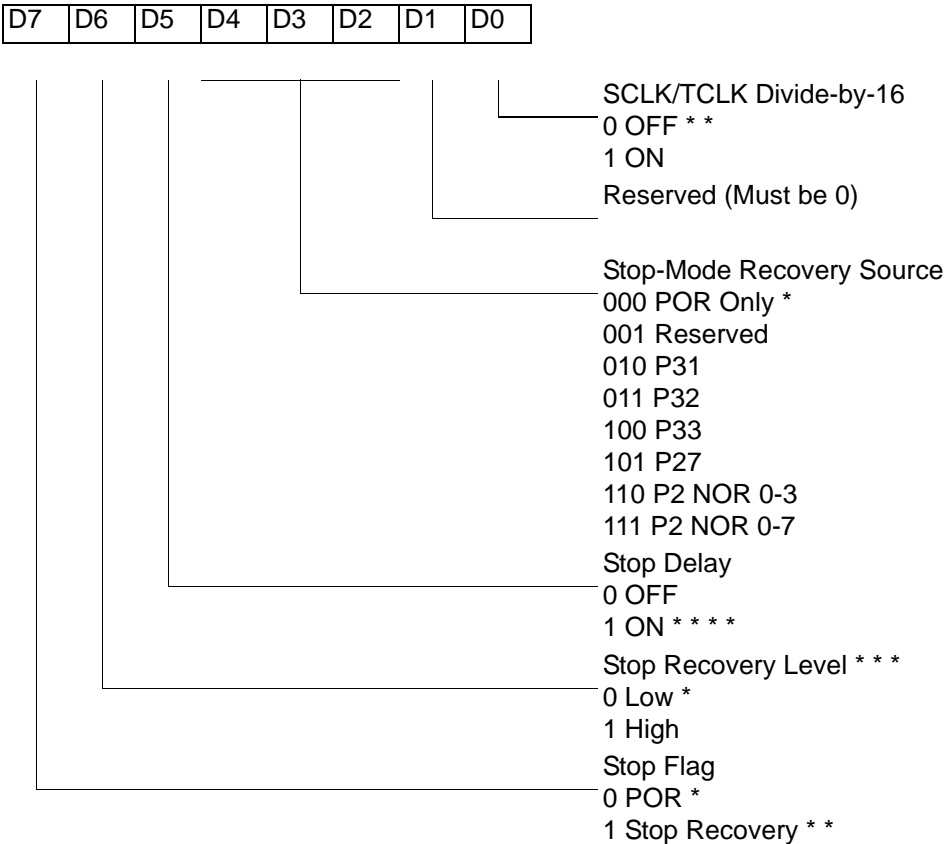
Stop-Mode Recovery

Stop-Mode Recovery Register (SMR)

This register selects the clock divide value and determines the mode of STOP mode Recovery ([Figure 32](#)). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of Stop recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level at the XOR-gate input ([Figure 34](#)) is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop-Mode Recovery signal. Bits D0 determines if SCLK/TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address 0BH.



SMR(0F)0Bh



* Default setting after reset
* * Default setting after reset and stop-mode recovery
* * * At the XOR gate input
* * * * Default setting after reset. Recommended to be set to 1 if using a crystal or resonator clock source.

Figure 32. STOP Mode Recovery Register

SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK (Figure 33). This control selectively reduces device power consumption during normal processor execution (SCLK control) and/or Halt Mode (where TCLK sources interrupt logic). After STOP mode Recovery, this bit is set to a 0.

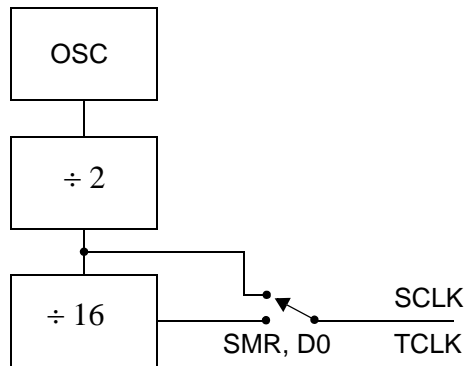


Figure 33. SCLK Circuit

Stop-Mode Recovery Source (D2, D3, and D4)

These three bits of the SMR specify the wake-up source of the Stop recovery (Figure 34 and Table 19).

Stop-Mode Recovery Register 2—SMR2(F)0Dh

Table 18 lists and briefly describes the fields for this register.

Table 18. SMR2(F)0Dh:STOP mode Recovery Register 2*

Field	Bit Position	Value	Description
Reserved	7-----	0	Reserved (Must be 0)
Recovery Level	-6-----	W 0 [†] 1	Low High
Reserved	--5-----	0	Reserved (Must be 0)
Source	---432--	W 000 [†] 001 010 011 100 101 110 111	A. POR Only B. NAND of P23–P20 C. NAND of P27–P20 D. NOR of P33–P31 E. NAND of P33–P31 F. NOR of P33–P31, P00, P07 G. NAND of P33–P31, P00, P07 H. NAND of P33–P31, P22–P20
Reserved	-----10	00	Reserved (Must be 0)

Notes:

* Port pins configured as outputs are ignored as an SMR recovery source.

[†] Indicates the value upon Power-On Reset

Figure 34. STOP Mode Recovery Source

Table 19. STOP Mode Recovery Source

SMR:432			Operation
D4	D3	D2	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	Reserved
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

- **Note:** Any Port 2 bit defined as an output drives the corresponding input to the default state. This condition allows the remaining inputs to control the AND/OR function. Refer to SMR2 register on page 58 for other recover sources.

STOP Mode Recovery Delay Select (D5)

This bit, if low, disables the T_{POR} delay after STOP mode recovery. The default configuration of this bit is 1. If the “fast” wake up is selected, the Stop-Mode Recovery source must be kept active for at least 10 T_{pC} .

- **Note:** This bit must be set to 1 if using a crystal or resonator clock source. The T_{POR} delay allows the clock source to stabilize before executing instructions.

STOP Mode Recovery Edge Select (D6)

A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the Crimzon™ ZLR32300 from STOP mode. A 0 indicates Low level recovery. The default is 0 on POR.

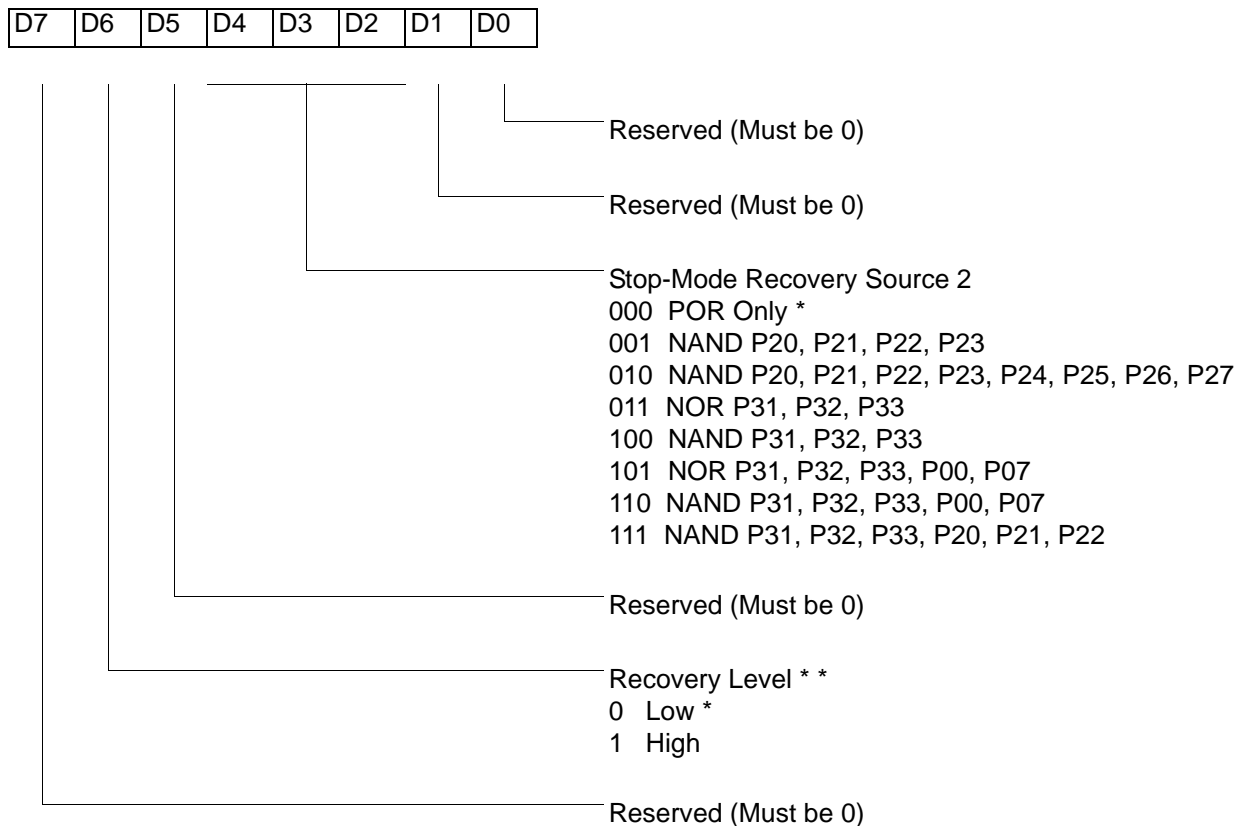
Cold or Warm Start (D7)

This bit is read only. It is set to 1 when the device is recovered from STOP mode. The bit is set to 0 when the device reset is other than STOP Mode Recovery (SMR).

STOP Mode Recovery Register 2 (SMR2)

This register determines the mode of STOP Mode Recovery for SMR2 (Figure 35).

SMR2(0F)Dh



Note: If used in conjunction with SMR, either of the two specified events causes a Stop-Mode Recovery.

* Default setting after reset

* * At the XOR gate input

Figure 35. STOP Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only)

If SMR2 is used in conjunction with SMR, either of the specified events causes a STOP mode Recovery.

- **Note:** Port pins configured as outputs are ignored as an SMR or SMR2 recovery source. For example, if the NAND or P23–P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23–P21) form the NAND equation.



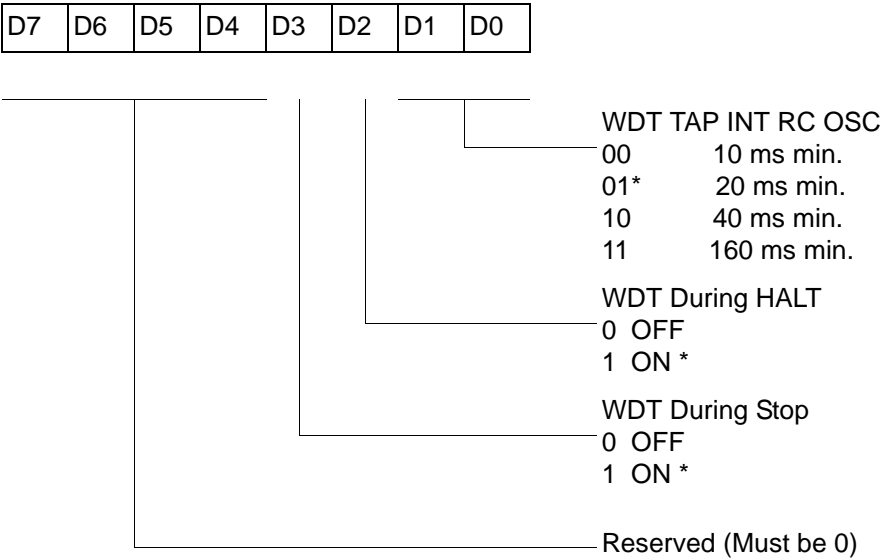
Watch-Dog Timer Mode

Watch-Dog Timer Mode Register (WDTMR)

The Watch-Dog Timer (WDT) is a retriggerable one-shot timer that resets the Z8® if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction. On subsequent executions of the WDT instruction, the WDT is refreshed. The WDT circuit is driven by an on-board RC-oscillator. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source the internal RC-oscillator. Bits 0 and 1 of the WDT register control a tap circuit that determines the minimum timeout period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during Stop. Bits 4 through 7 are reserved (Figure 36). This register is accessible only during the first 60 processor cycles (120 XTAL clocks) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset, or a Stop-Mode Recovery (Figure 35). After this point, the register cannot be modified by any means (intentional or otherwise). The WDTMR cannot be read. The register is located in Bank F of the Expanded Register Group at address location 0Fh. It is organized as shown in Figure 36.

WDTMR(0F)0Fh



* Default setting after reset

Figure 36. WATCH-DOG TIMER Mode Register (Write Only)

WDT Time Select (D0, D1)

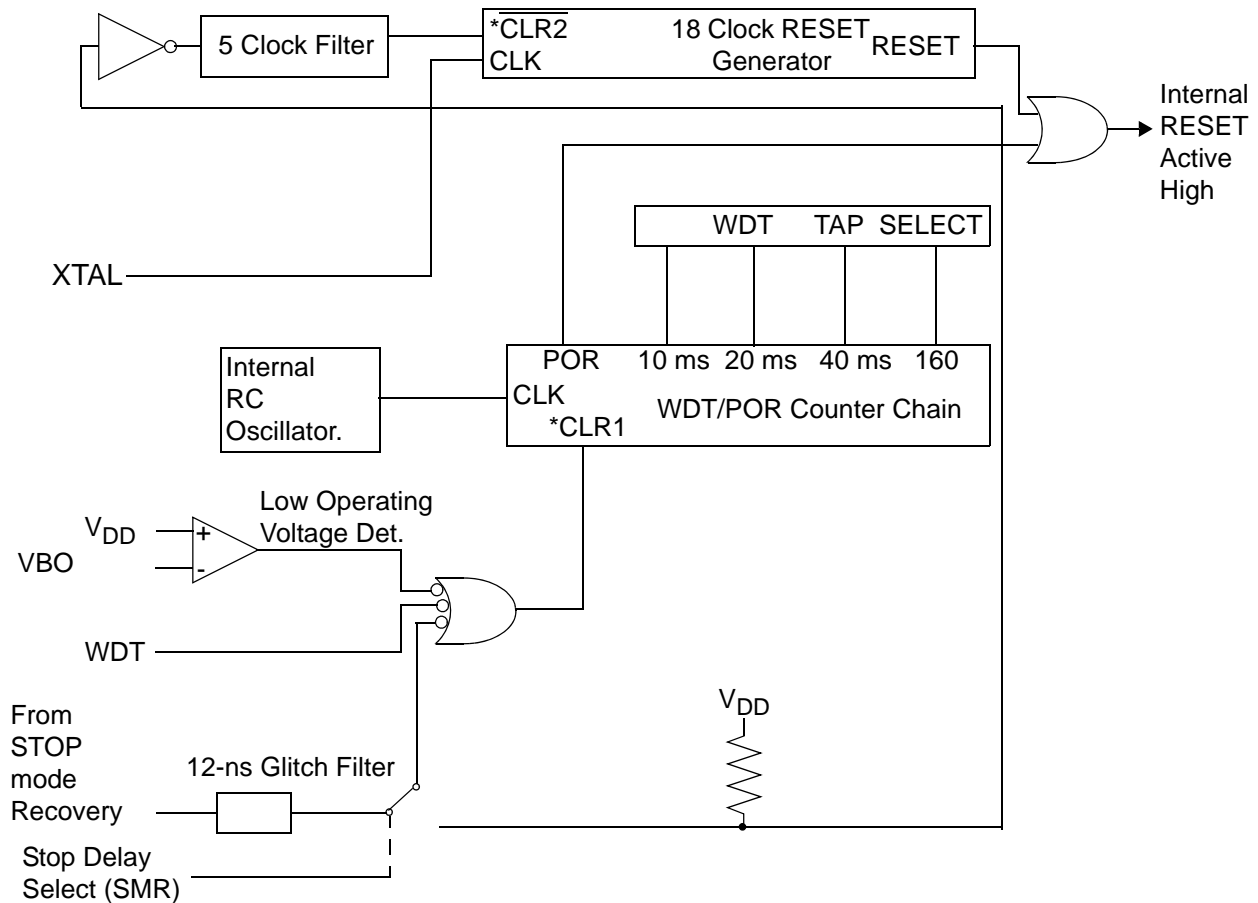
This bit selects the WDT time period. It is configured as indicated in [Table 20](#).

Table 20. Watch-Dog Timer Time Select

D1	D0	Timeout of Internal RC-Oscillator
0	0	10ms min.
0	1	20ms min.
1	0	40ms min.
1	1	160ms min.

WDTMR During Halt (D2)

This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1. See [Figure 37](#).



* CLR1 and $\overline{\text{CLR2}}$ enable the WDT/POR and 18 Clock Reset timers respectively upon a Low-to-High input translation.

Figure 37. Resets and WDT

WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. A 1 indicates active during Stop. The default is 1.

ROM Selectable Options

There are seven ROM Selectable Options to choose from based on ROM code requirements. These are listed in [Table 21](#).

Table 21. ROM Selectable Options

Port 00–03 Pull-Ups	On/Off
Port 04–07 Pull-Ups	On/Off
Port 10–13 Pull-Ups	On/Off
Port 14–17 Pull-Ups	On/Off
Port 20–27 Pull-Ups	On/Off
Port 3 Pull-Ups	On/Off
Watch-Dog Timer at Power-On Reset	On/Off

Voltage Brown-Out/Standby

An on-chip Voltage Comparator checks that the V_{DD} is at the required level for correct operation of the device. Reset is globally driven when V_{DD} falls below V_{BO} . A small drop in V_{DD} causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the V_{DD} is allowed to stay above V_{RAM} , the RAM content is preserved. When the power level is returned to above V_{BO} , the device performs a POR and functions normally.

Low-Voltage Detection**Low-Voltage Detection Register—LVD(D)0CH**

- **Note:** Voltage detection does not work at STOP mode. It must be disabled during STOP mode in order to reduce current.

Field	Bit Position	Description
LVD	76543---	Reserved No Effect
	----2--	R 1 HVD flag set 0* HVD flag reset
	-----1-	R 1 LVD flag set 0* LVD flag reset
	-----0	R/W 1 Enable VD 0* Disable VD
*Default after POR		

- **Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

Voltage Detection and Flags

The Voltage Detection register (LVD, register 0Ch at the expanded register bank 0Dh) offers an option of monitoring the V_{CC} voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the V_{CC} level is monitored in real time. The flags in the LVD register valid 20uS after Voltage Detection is enabled. The HVD flag (bit 2 of the LVD register) is set only if V_{CC} is higher than V_{HVD} . The LVD flag (bit 1 of the LVD register) is set only if V_{CC} is lower than the V_{LVD} . When Voltage Detection is enabled, the LVD flag also triggers IRQ5. The IRQ bit 5 latches the low voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a flag only.

- **Note:** If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt instruction (EI) prior to enabling the voltage detection.

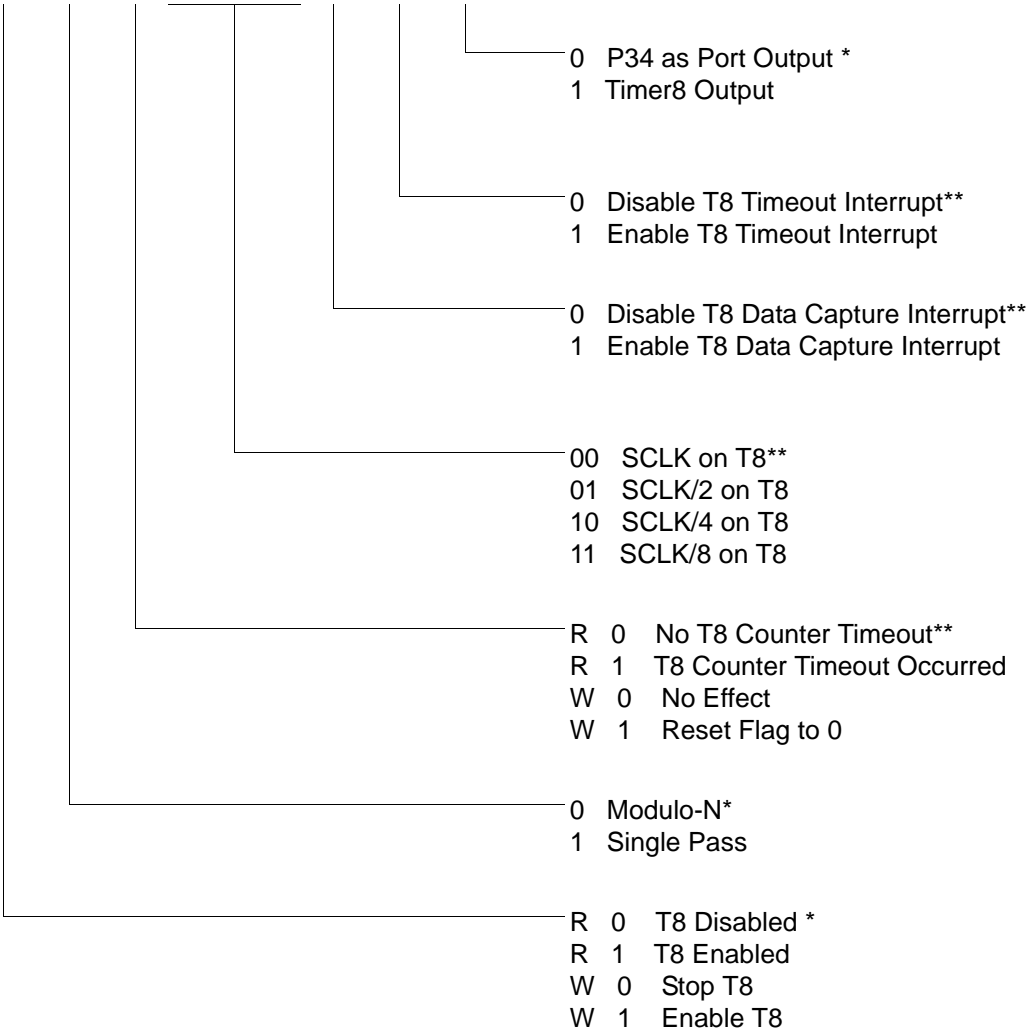
Expanded Register File Control Registers (0D)

The expanded register file control registers (0D) are depicted in [Figures 38 through Figure 42](#).



CTR0(0D)00h

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



* Default setting after reset
**Default setting after reset. Not reset with a Stop Mode recovery.

Figure 38. TC8 Control Register ((0D)00H: Read/Write Except Where Noted)

CTR1(0D)01h

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

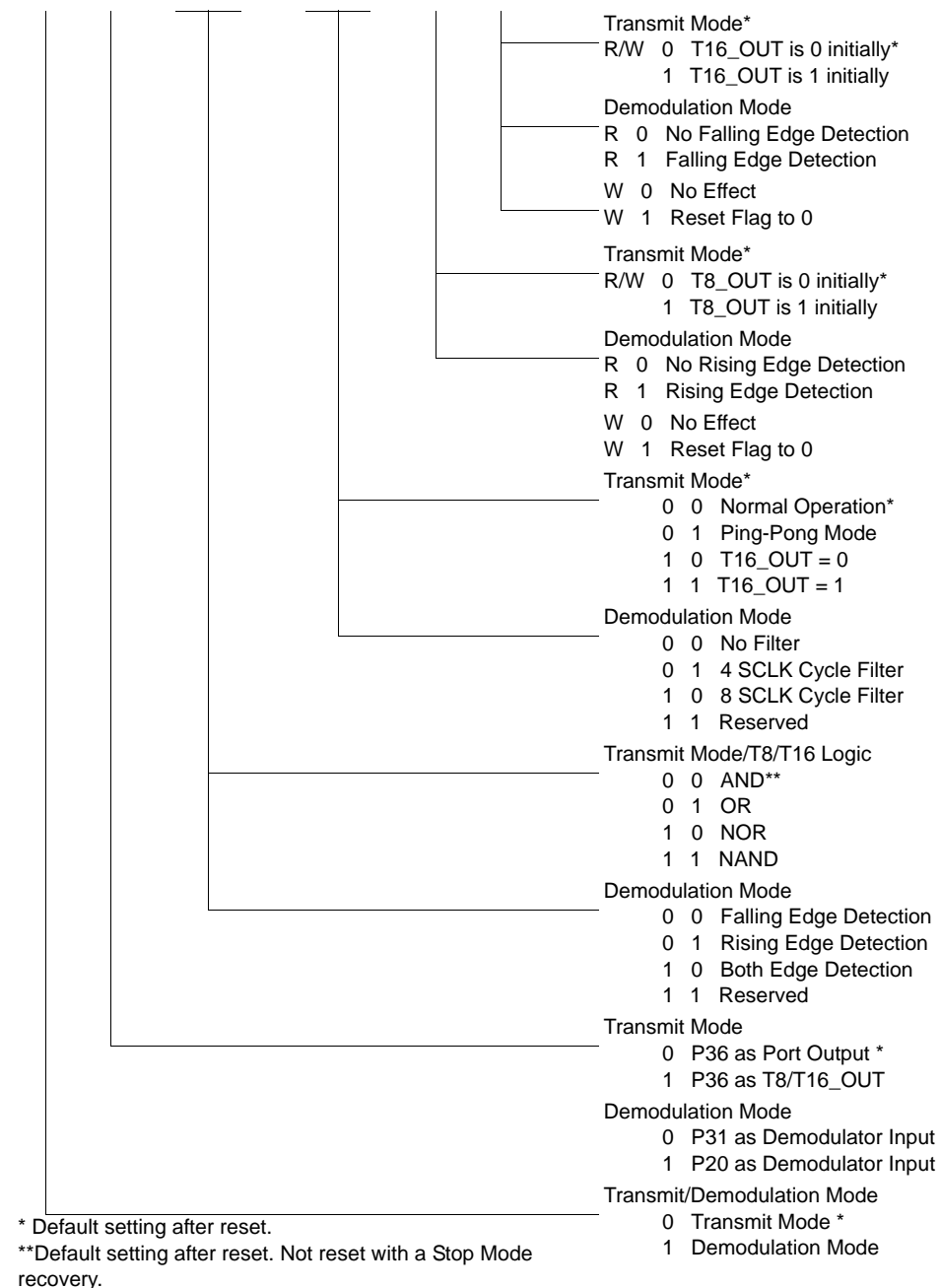


Figure 39. T8 and T16 Common Control Functions ((0D)01H: Read/Write)

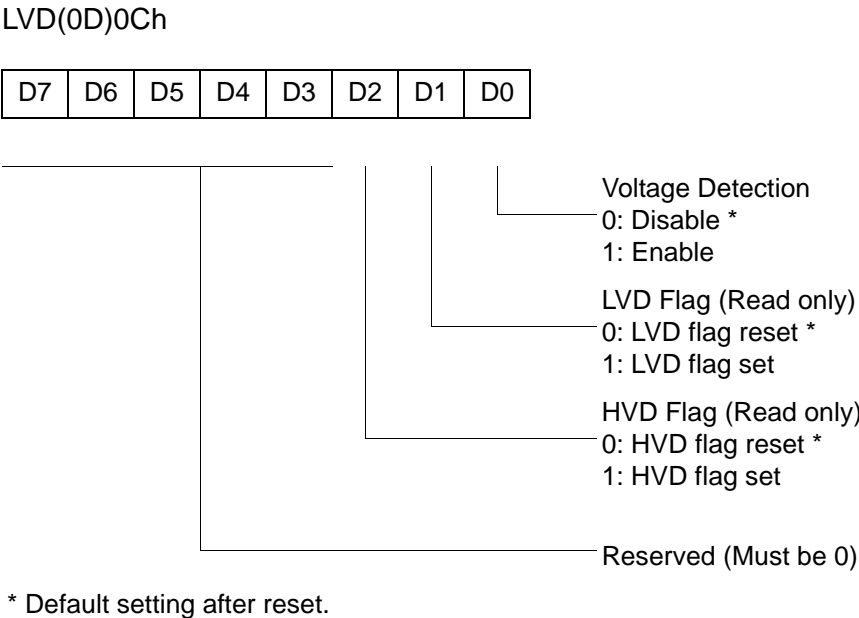


Figure 42. Voltage Detection Register

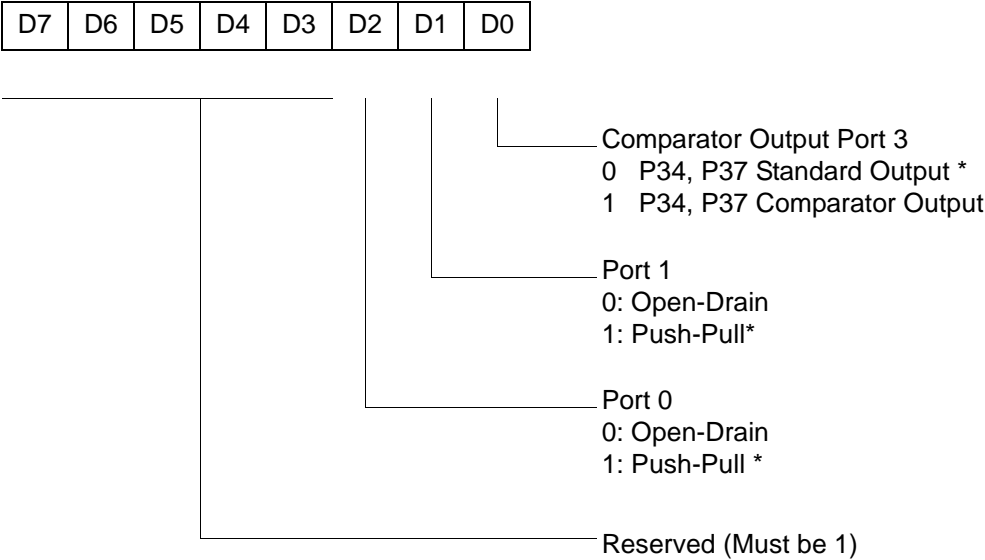
► **Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

Expanded Register File Control Registers (0F)

The expanded register file control registers (0F) are depicted in [Figures 43 through Figure 56](#).



PCON(0F)00h

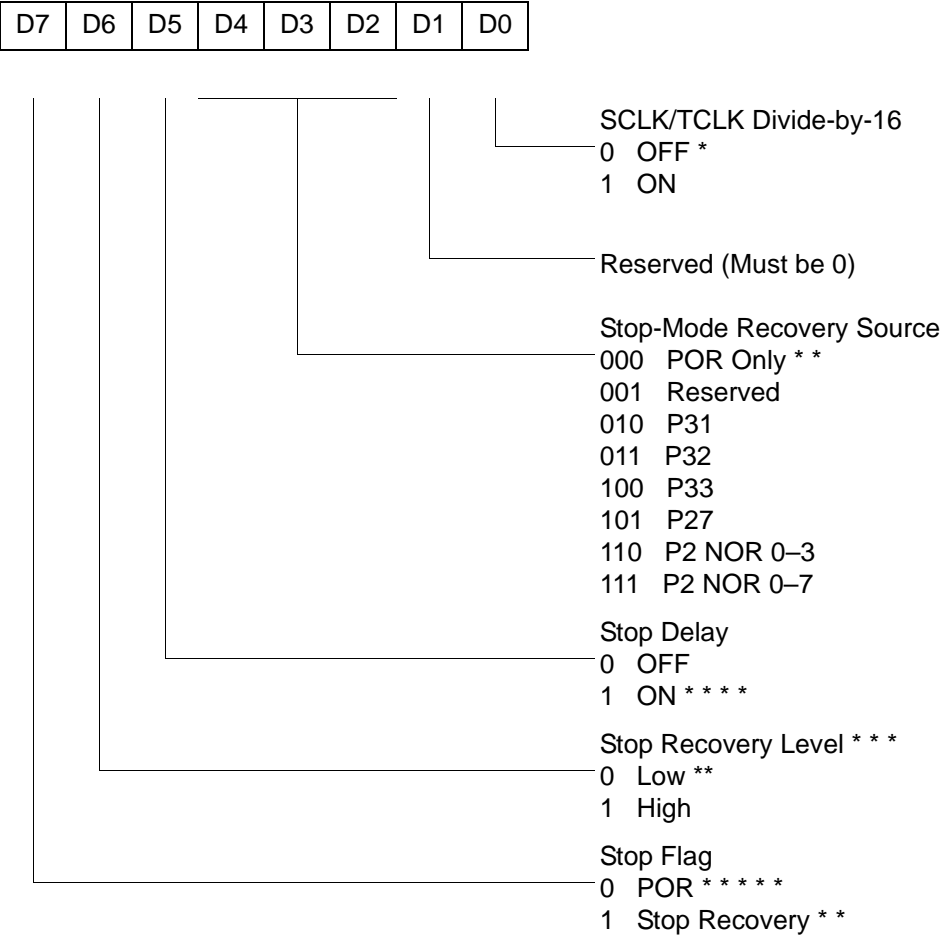


* Default setting after reset

Figure 43. Port Configuration Register (PCON)(0F)00H: Write Only)

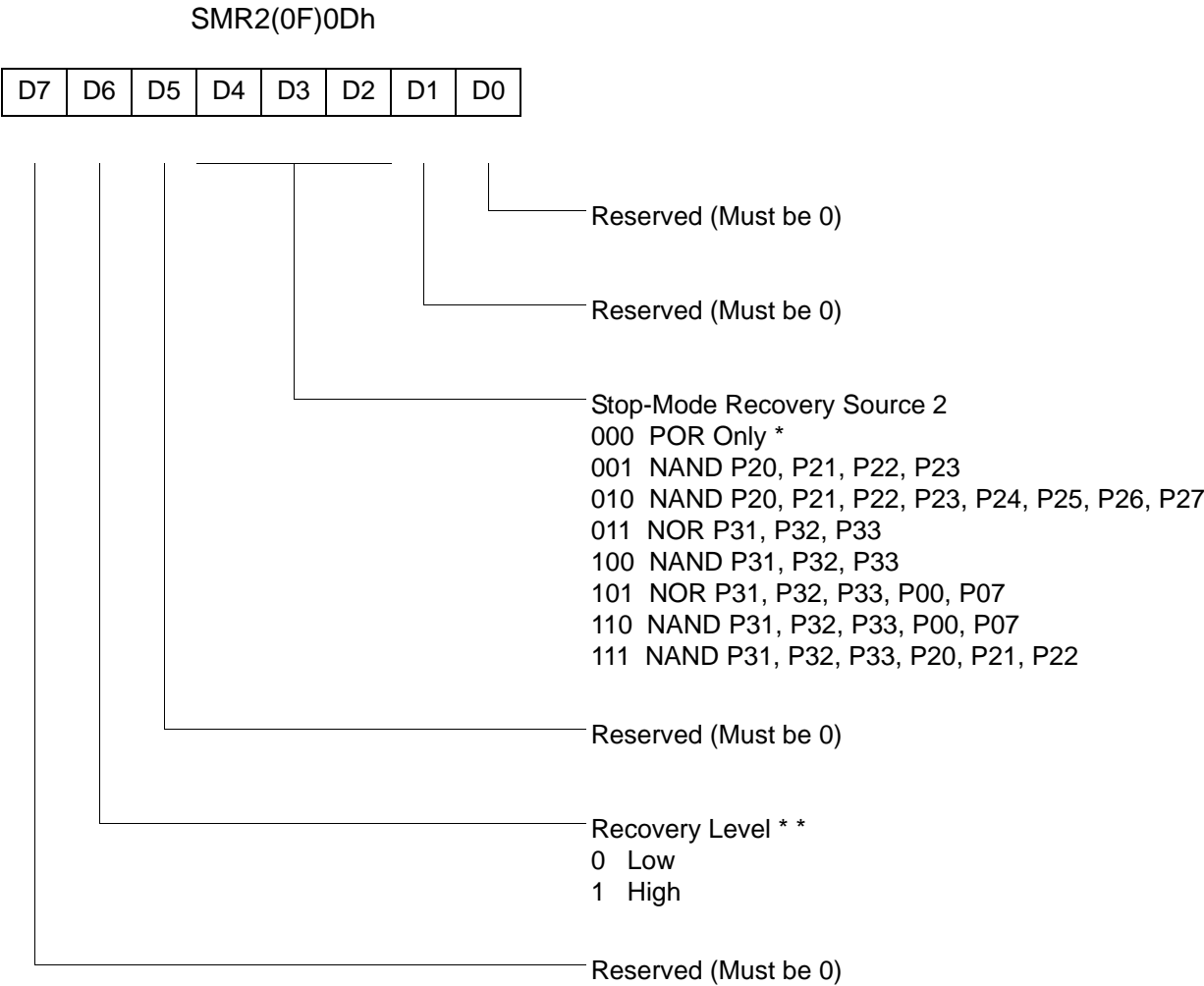


SMR(0F)0Bh



- * Default setting after reset
- ** Default setting after reset and stop-mode recovery
- *** At the XOR gate input
- **** Default setting after reset. Recommended to be set to 1 if using a crystal or resonator clock source. Not reset with Stop Mode recovery.
- ***** Default setting after Power-On Reset.

Figure 44. STOP mode Recovery Register ((0F)0BH: D6–D0=Write Only, D7=Read Only)

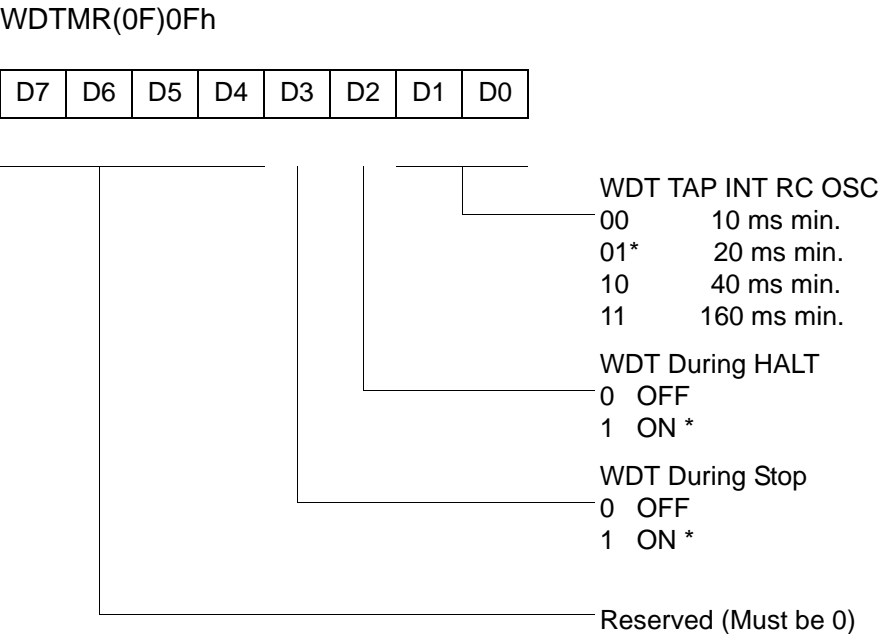


Note: If used in conjunction with SMR, either of the two specified events causes a Stop-Mode Recovery.

* Default setting after reset. Not reset with a Stop Mode recovery.

* * At the XOR gate input

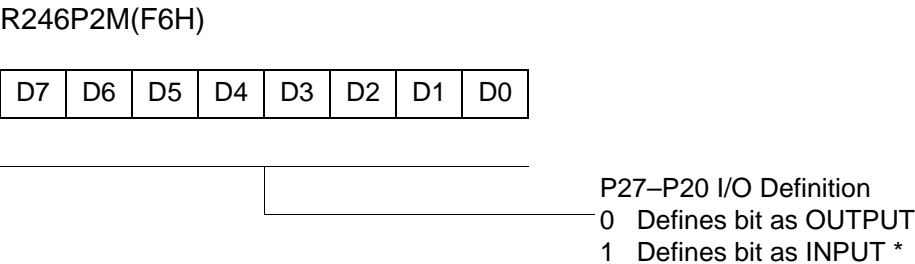
Figure 45. STOP mode Recovery Register 2 ((0F)0DH:D2–D4, D6 Write Only)



* Default setting after reset. Not reset wit a Stop Mode recovery.

Figure 46. Watch-Dog Timer Register ((0F) 0FH: Write Only)

Standard Control Registers



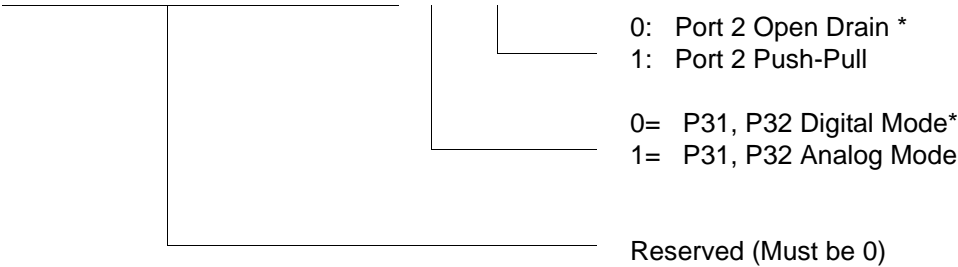
* Default setting after reset. Not reset wit a Stop Mode recovery.

Figure 47. Port 2 Mode Register (F6H: Write Only)



R247P3M(F7H)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

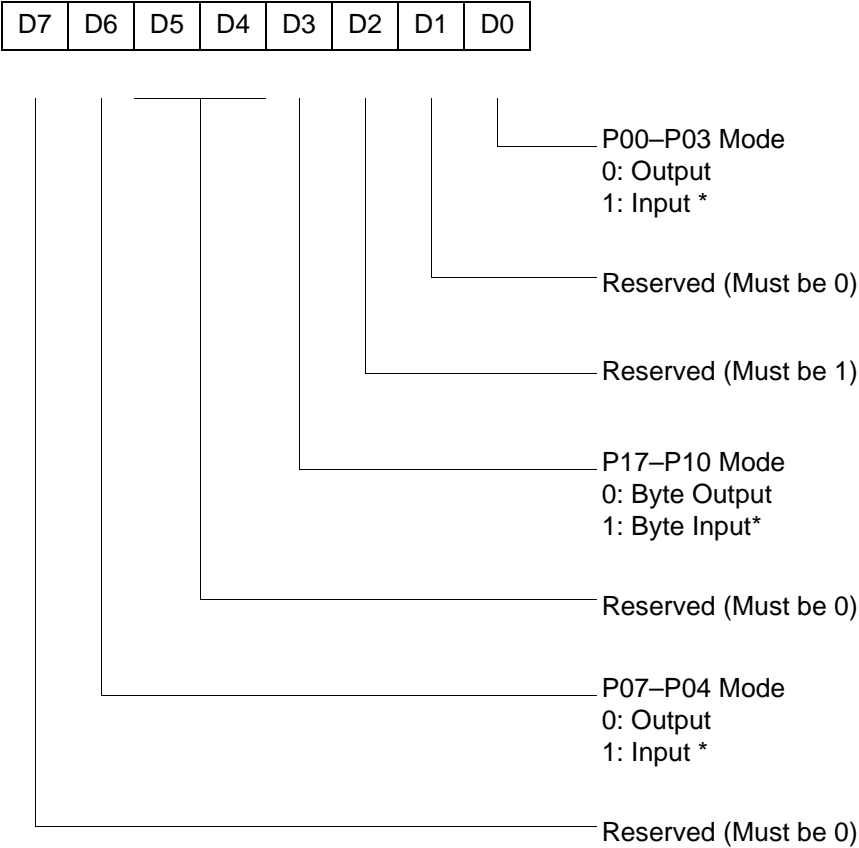


* Default setting after reset. Not reset wit a Stop Mode recovery.

Figure 48. Port 3 Mode Register (F7H: Write Only)



R248 P01M(F8H)



* Default setting after reset; only P00, P01 and P07 are available on Crimzon™ ZLR32300 20-pin configurations.

Figure 49. Port 0 and 1 Mode Register (F8H: Write Only)



R249 IPR(F9H)

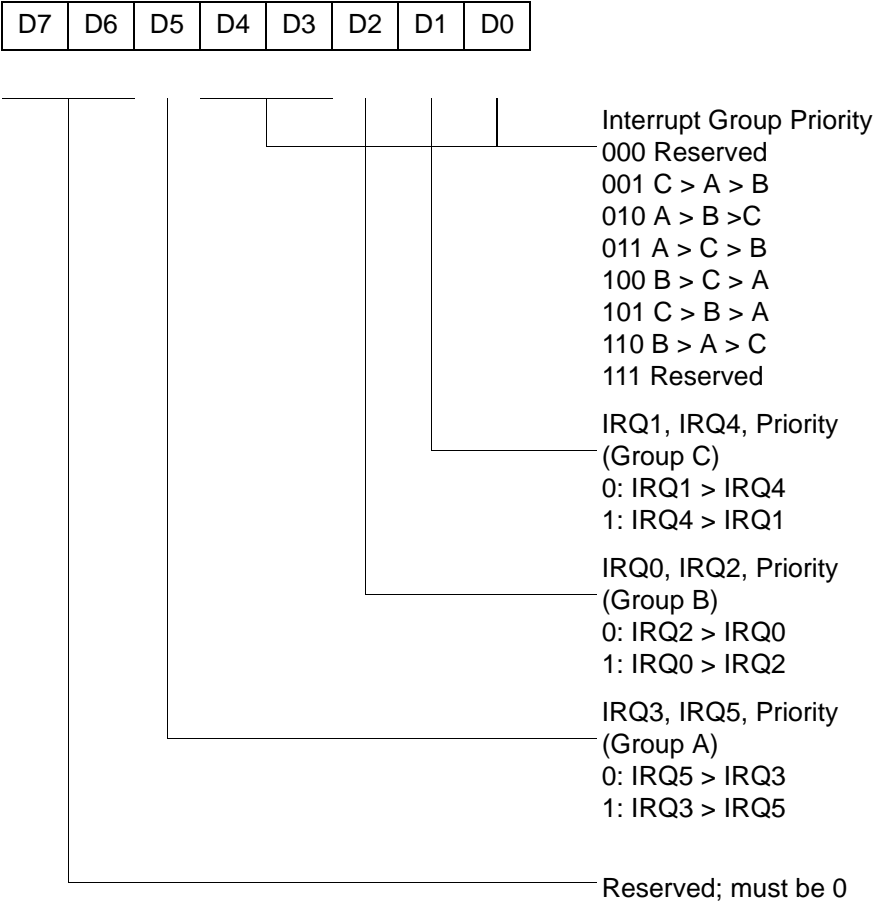


Figure 50. Interrupt Priority Register (F9H: Write Only)



R250 IRQ(FAH)

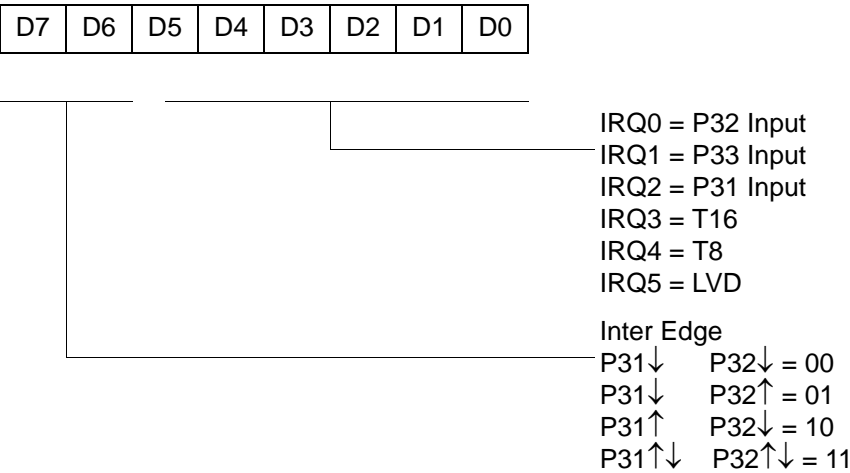


Figure 51. Interrupt Request Register (FAH: Read/Write)

R251 IMR(FBH)



* Default setting after reset
** Only by using EI, DI instruction; DI is required before changing the IMR register

Figure 52. Interrupt Mask Register (FBH: Read/Write)



R252 Flags(FCH)

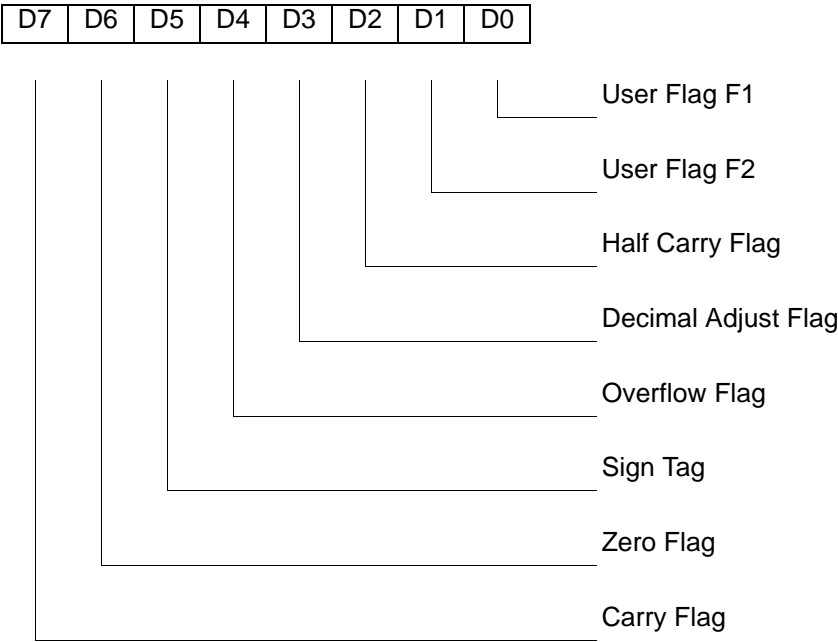
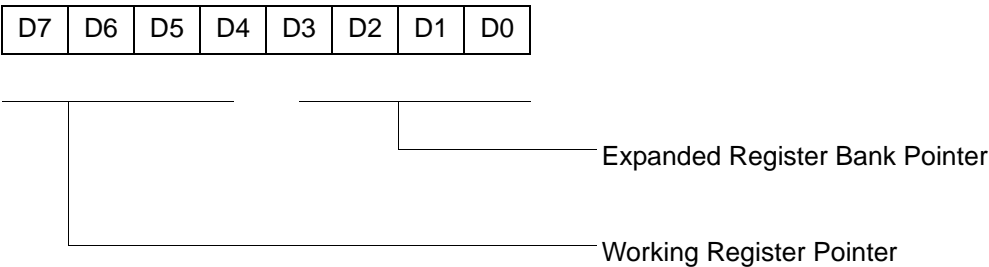


Figure 53. Flag Register (FCH: Read/Write)

R253 RP(FDH)



Default setting after reset = 0000 0000

Figure 54. Register Pointer (FDH: Read/Write)

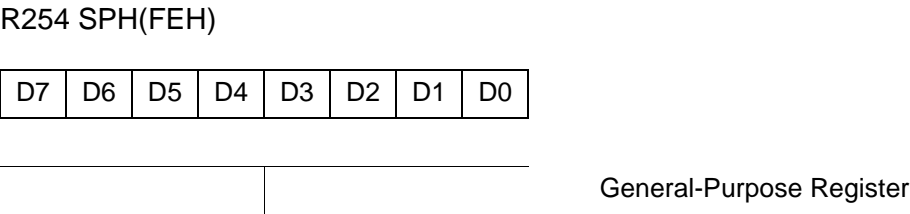


Figure 55. Stack Pointer High (FEH: Read/Write)

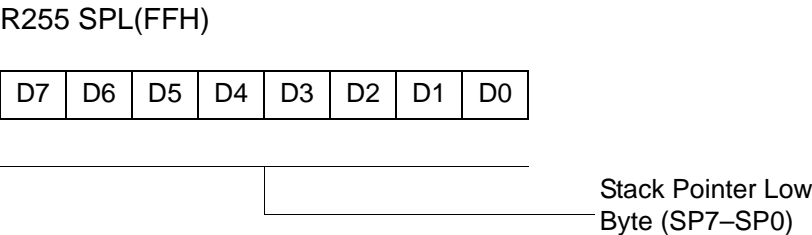
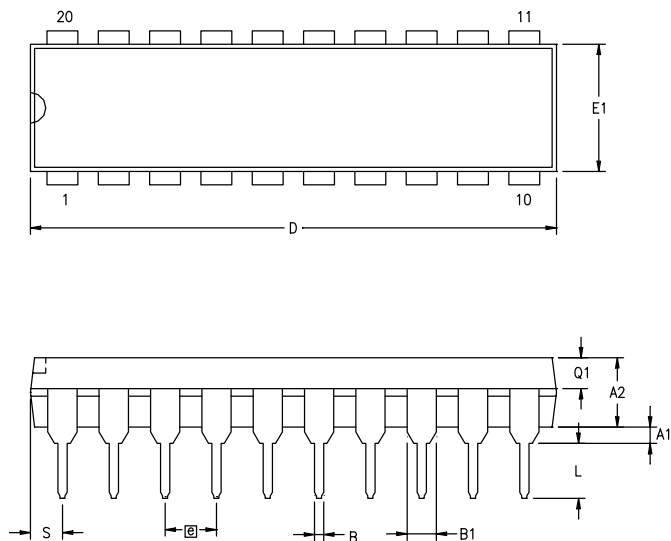


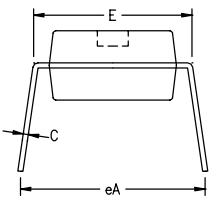
Figure 56. Stack Pointer Low (FFH: Read/Write)

Package Information

Package information for all versions of Crimzon™ ZLR32300 is depicted in [Figures 57 through Figure 63](#).

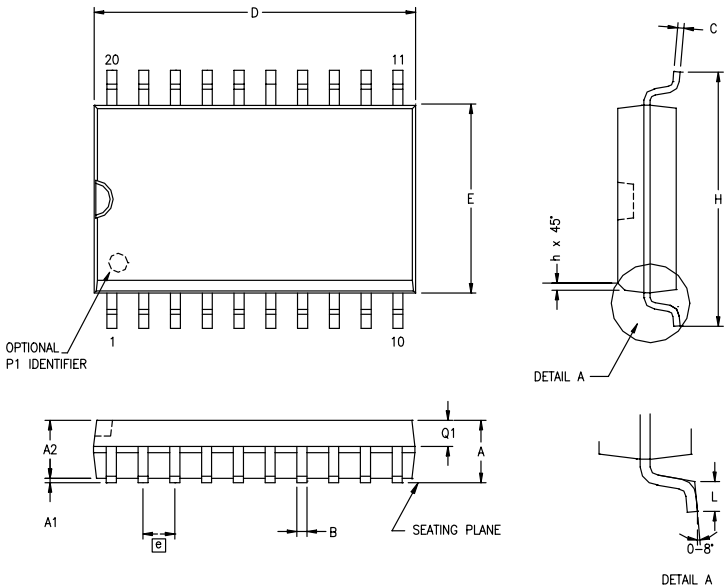


SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.38	0.81	.015	.032
A2	3.25	3.68	.128	.145
B	0.41	0.51	.016	.020
B1	1.47	1.57	.058	.062
C	0.20	0.30	.008	.012
D	25.65	26.16	1.010	1.030
E	7.49	8.26	.295	.325
E1	6.10	6.65	.240	.262
Ⓢ	2.54 BSC		.100 BSC	
eA	7.87	9.14	.310	.360
L	3.18	3.43	.125	.135
Q1	1.42	1.65	.056	.065
S	1.52	1.65	.060	.065



CONTROLLING DIMENSIONS : INCH

Figure 57. 20-Pin PDIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	12.60	12.95	.496	.510
E	7.40	7.60	.291	.299
Ⓢ	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 58. 20-Pin SOIC Package Diagram

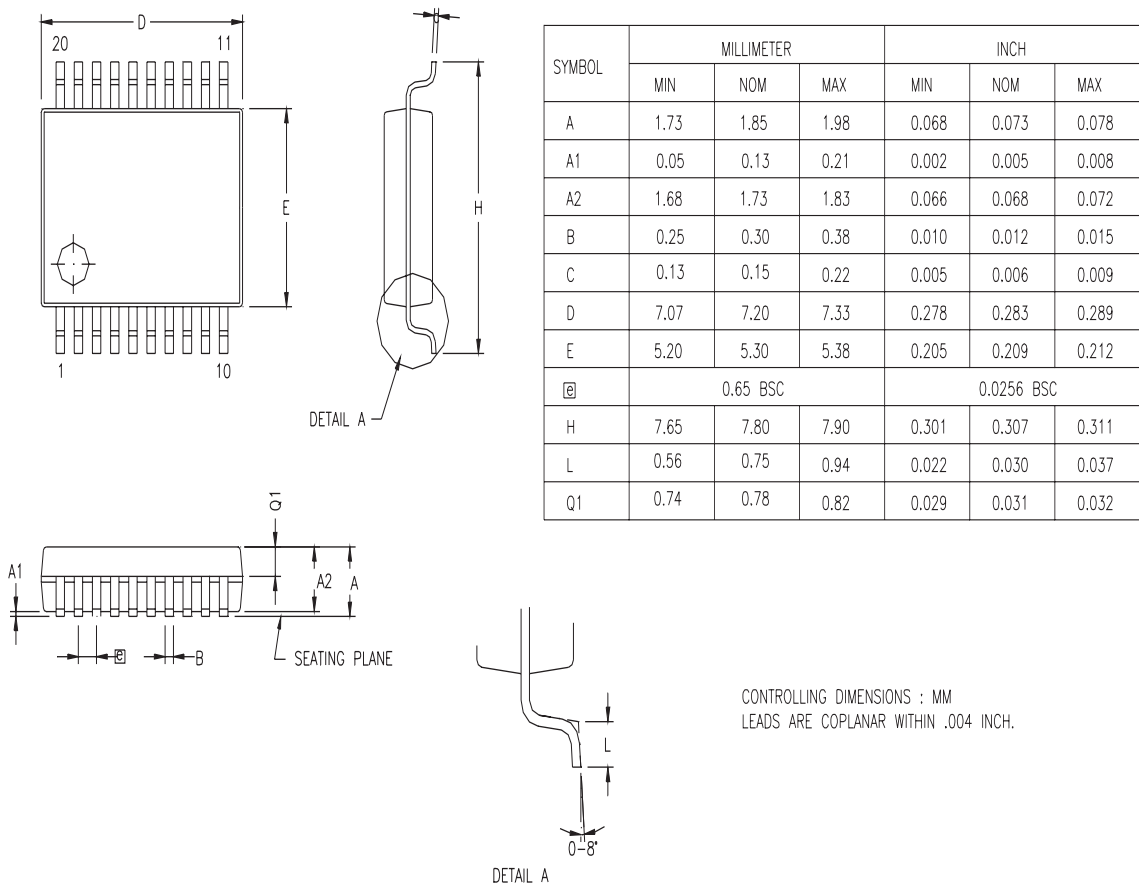


Figure 59. 20-Pin SSOP Package Diagram

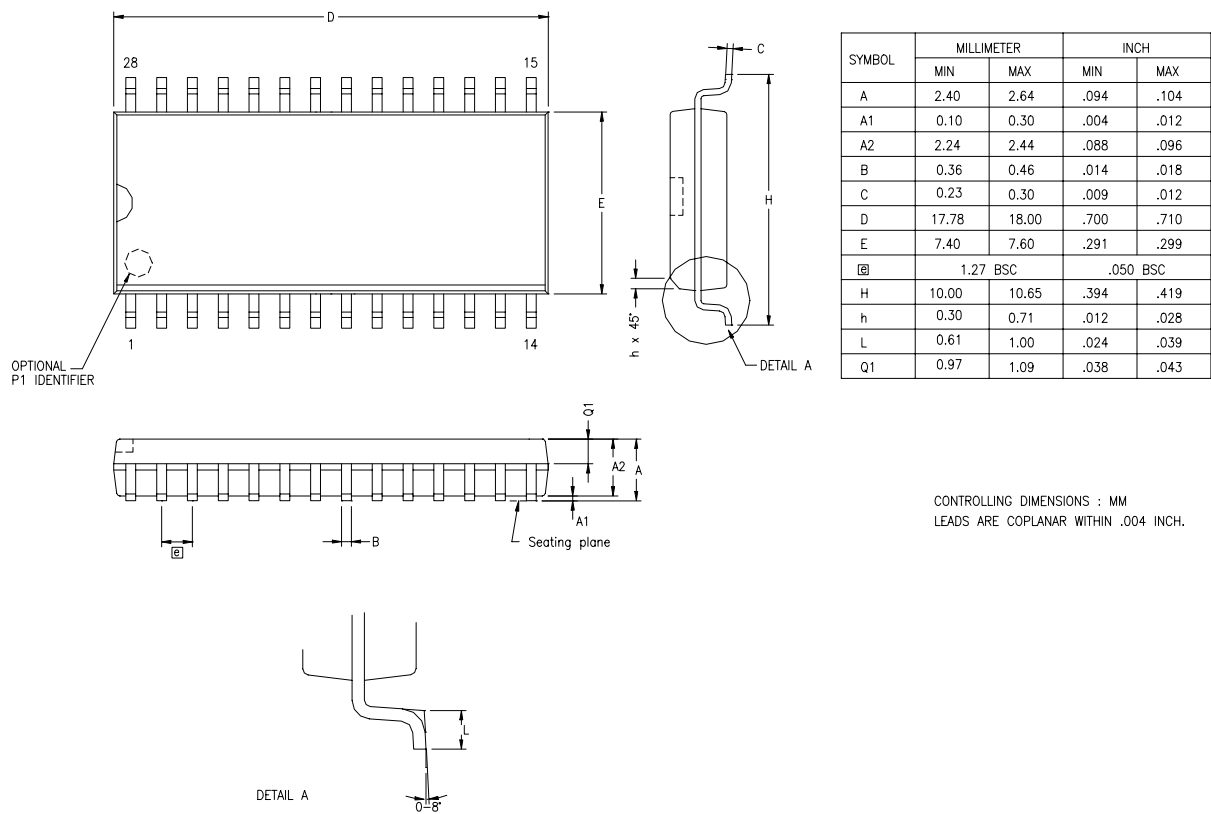
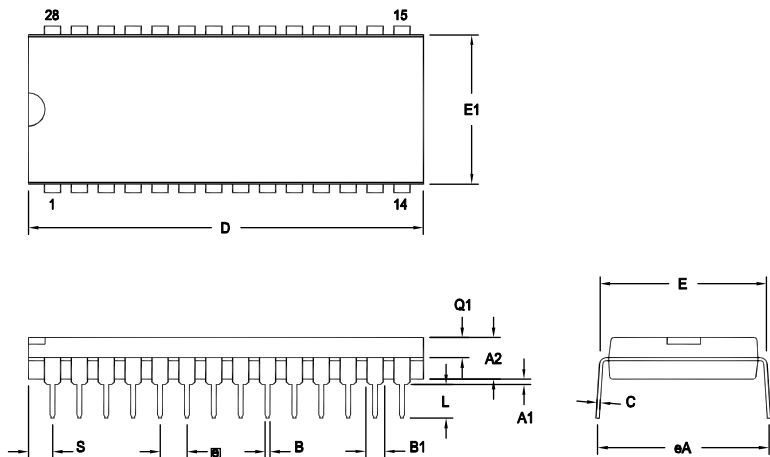


Figure 60. 28-Pin SOIC Package Diagram



OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

Note: ZILOG supplies both options for production. Component layout
PCB design should cover bigger option 01.

SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.38	1.02	.015	.040
A2		3.18	4.19	.125	.165
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 BSC	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.40	1.91	.055	.075
	02	1.40	1.78	.055	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

CONTROLLING DIMENSIONS : INCH

Figure 61. 28-Pin PDIP Package Diagram

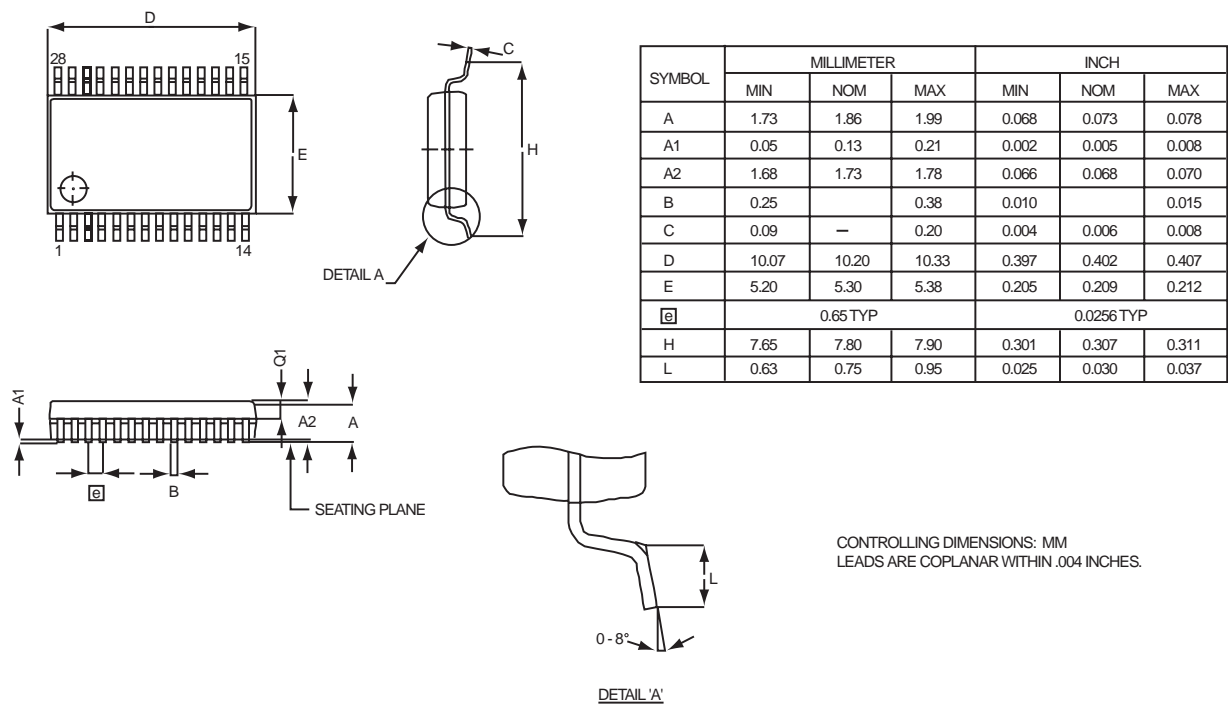
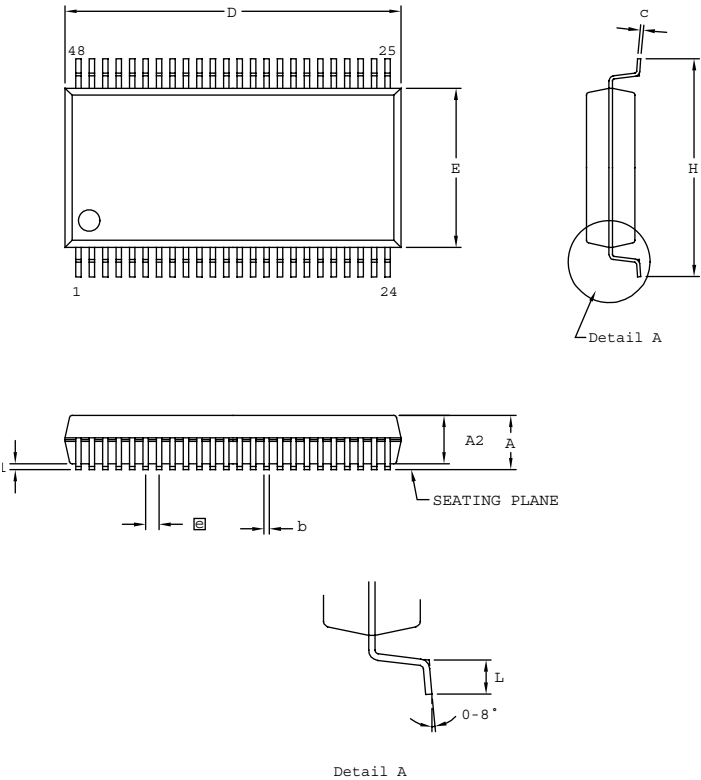


Figure 62. 28-Pin SSOP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.41	2.79	0.095	0.110
A1	0.23	0.38	0.009	0.015
A2	2.18	2.39	0.086	0.094
b	0.20	0.34	0.008	0.0135
c	0.13	0.25	0.005	0.010
D	15.75	16.00	0.620	0.630
E	7.39	7.59	0.291	0.299
⌀	0.635 BSC		0.025 BSC	
H	10.16	10.41	0.400	0.410
L	0.51	1.016	0.020	0.040

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH

Figure 63. 48-Pin SSOP Package Design

► **Note:** Please check with ZiLOG on the actual bonding diagram and coordinate for chip-on-board assembly.

Ordering Information

Memory Size	Part Number	Description
32K		
	ZLR32300H4832G	48-pin SSOP 32K ROM
	ZLR32300H2832G	28-pin SSOP 32K ROM
	ZLR32300P2832G	28-pin PDIP 32K ROM
	ZLR32300S2832G	28-pin SOIC 32K ROM
	ZLR32300H2032G	20-pin SSOP 32K ROM
	ZLR32300P2032G	20-pin PDIP 32K ROM
	ZLR32300S2032G	20-pin SOIC 32K ROM
24K		
	ZLR32300H4824G	48-pin SSOP 24K ROM
	ZLR32300H2824G	28-pin SSOP 24K ROM
	ZLR32300P2824G	28-pin PDIP 24K ROM
	ZLR32300S2824G	28-pin SOIC 24K ROM
	ZLR32300H2024G	20-pin SSOP 24K ROM
	ZLR32300P2024G	20-pin PDIP 24K ROM
	ZLR32300S2024G	20-pin SOIC 24K ROM
16K		
	ZLR32300H4816G	48-pin SSOP 16K ROM
8K		
	ZLR32300H4808G	48-pin SSOP 8K ROM
4K		
	ZLR32300H4804G	48-pin SSOP 4K ROM
	ZLP128ICE01ZEM	In-Circuit Emulator
	ZLP323ICE01ZAC	40-PDIP/48-SSOP Accessory Kit

Note:
Contact www.zilog.com for the die form.



For fast results, contact your local ZiLOG sales office for assistance in ordering the part desired.

Part Number Description

ZiLOG part numbers consist of a number of components, as shown in [Figure 64](#). The example part number ZLR32300H2832G is a Crimzon™ masked ROM product in a 28-pin SSOP package, with 32 KB of ROM and built with lead-free solder.

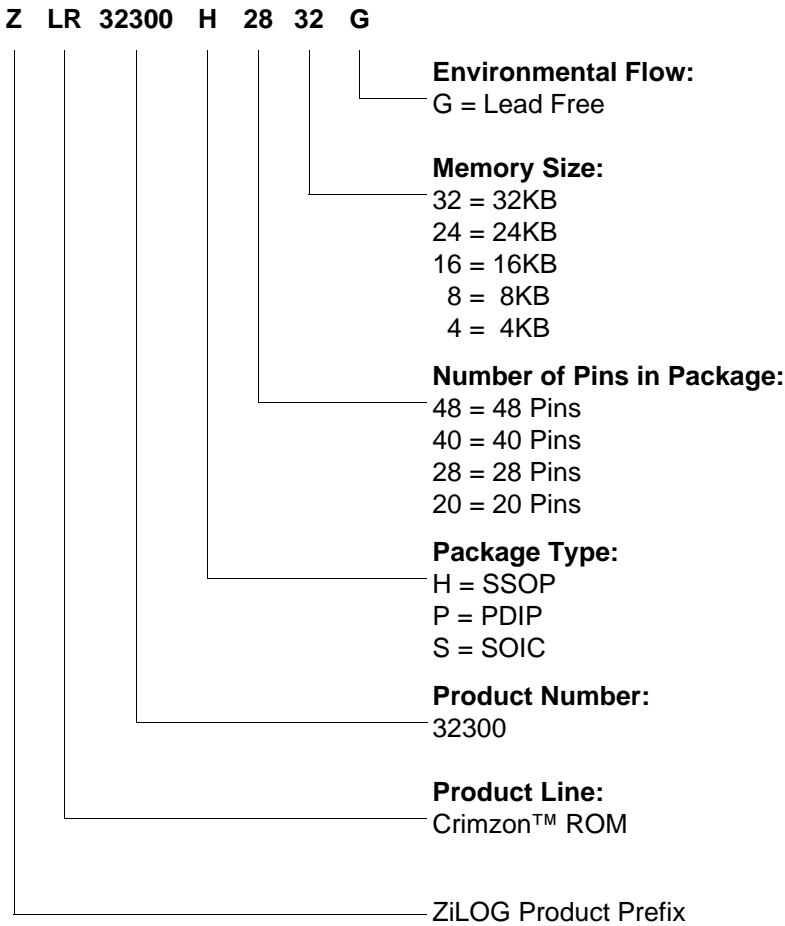


Figure 64. Part Number Description Example

Index

Numerics

- 16-bit counter/timer circuits 43
- 20-pin DIP package diagram 79
- 20-pin SSOP package diagram 80
- 28-pin DIP package diagram 82
- 28-pin SOIC package diagram 81
- 28-pin SSOP package diagram 83
- 40-pin DIP package diagram 83
- 48-pin SSOP package diagram 84
- 8-bit counter/timer circuits 39

A

- absolute maximum ratings 10
- AC
 - characteristics 13
 - timing diagram 13
- address spaces, basic 2
- architecture 2
 - expanded register file 25

B

- basic address spaces 2
- block diagram, ZLP32300 functional 4

C

- capacitance 11
- characteristics
 - AC 13
 - DC 11
- clock 50
- comparator inputs/outputs 22
- configuration
 - port 0 16
 - port 1 17
 - port 2 18
 - port 3 19
 - port 3 counter/timer 21

counter/timer

- 16-bit circuits 43
- 8-bit circuits 39
- brown-out voltage/standby 61
- clock 50
- demodulation mode count capture flow-chart 41
- demodulation mode flowchart 42
- diagram 3
- EPROM selectable options 61
- glitch filter circuitry 37
- halt instruction 51
- input circuit 37
- interrupt block diagram 48
- interrupt types, sources and vectors 49
- oscillator configuration 50
- output circuit 46
- ping-pong mode 45
- port configuration register 52
- resets and WDT 61
- SCLK circuit 55
- stop instruction 51
- stop mode recovery register 54
- stop mode recovery register 2 58
- stop mode recovery source 56
- T16 demodulation mode 44
- T16 transmit mode 43
- T16_OUT in modulo-N mode 44
- T16_OUT in single-pass mode 44
- T8 demodulation mode 40
- T8 transmit mode 37
- T8_OUT in modulo-N mode 40
- T8_OUT in single-pass mode 40
- transmit mode flowchart 38
- voltage detection and flags 62
- watch-dog timer mode register 59
- watch-dog timer time select 60

CTR(D)01h T8 and T16 Common Functions 32

D

- DC characteristics 11
- demodulation mode
 - count capture flowchart 41
 - flowchart 42
 - T16 44
 - T8 40
- description
 - functional 22
 - general 2
 - pin 4

E

- EPROM
 - selectable options 61
- expanded register file 23
- expanded register file architecture 25
- expanded register file control registers 68
 - flag 77
 - interrupt mask register 76
 - interrupt priority register 75
 - interrupt request register 76
 - port 0 and 1 mode register 74
 - port 2 configuration register 72
 - port 3 mode register 73
 - port configuration register 72
 - register pointer 77
 - stack pointer high register 78
 - stack pointer low register 78
 - stop-mode recovery register 70
 - stop-mode recovery register 2 71
 - T16 control register 66
 - T8 and T16 common control functions register 64
 - T8/T16 control register 67
 - TC8 control register 62
 - watch-dog timer register 72

F

- features
 - standby modes 1

ZLP32300 1

- functional description
 - counter/timer functional blocks 37
 - CTR(D)01h register 32
 - CTR0(D)00h register 30
 - CTR2(D)02h register 34
 - CTR3(D)03h register 36
 - expanded register file 23
 - expanded register file architecture 25
 - HI16(D)09h register 29
 - HI8(D)0Bh register 29
 - LO8(D)0Ah register 29
 - LO16(D)08h register 29
 - program memory map 23
 - RAM 22
 - register description 62
 - register file 27
 - register pointer 26
 - register pointer detail 28
 - SMR2(F)0D1h register 37
 - stack 28
 - TC16H(D)07h register 29
 - TC16L(D)06h register 30
 - TC8H(D)05h register 30
 - TC8L(D)04h register 30

G

- glitch filter circuitry 37

H

- halt instruction, counter/timer 51

I

- input circuit 37
- interrupt block diagram, counter/timer 48
- interrupt types, sources and vectors 49

L

- low-voltage detection register 62



M

memory, program 22
modulo-N mode
 T16_OUT 44
 T8_OUT 40

O

oscillator configuration 50
output circuit, counter/timer 46

P

package information
 20-pin DIP package diagram 79
 20-pin SSOP package diagram 80
 28-pin DIP package diagram 82
 28-pin SOIC package diagram 81
 28-pin SSOP package diagram 83
 40-pin DIP package diagram 83
 48-pin SSOP package diagram 84
pin configuration
 20-pin DIP/SOIC/SSOP 5
 28-pin DIP/SOIC/SSOP 6
 40- and 48-pin 8
 40-pin DIP 7
 48-pin SSOP 8
pin functions
 port 0 (P07 - P00) 15
 port 0 (P17 - P10) 16
 port 0 configuration 16
 port 1 configuration 17
 port 2 (P27 - P20) 17
 port 2 (P37 - P30) 18
 port 2 configuration 18
 port 3 configuration 19
 port 3 counter/timer configuration 21
 reset) 22
 XTAL1 (time-based input 15
 XTAL2 (time-based output) 15
ping-pong mode 45
port 0 configuration 16
port 0 pin function 15

port 1 configuration 17
port 1 pin function 16
port 2 configuration 18
port 2 pin function 17
port 3 configuration 19
port 3 pin function 18
port 3 counter/timer configuration 21
port configuration register 52
power connections 3
power supply 5
precharacterization product 87
program memory 22
 map 23

R

ratings, absolute maximum 10
register 58
 CTR(D)01h 32
 CTR0(D)00h 30
 CTR2(D)02h 34
 CTR3(D)03h 36
 flag 77
 HI16(D)09h 29
 HI8(D)0Bh 29
 interrupt priority 75
 interrupt request 76
 interruptmask 76
 L016(D)08h 29
 L08(D)0Ah 29
 LVD(D)0Ch 62
 pointer 77
 port 0 and 1 74
 port 2 configuration 72
 port 3 mode 73
 port configuration 52, 72
 SMR2(F)0Dh 37
 stack pointer high 78
 stack pointer low 78
 stop mode recovery 54
 stop mode recovery 2 58, 71
 stop-mode recovery 70
 T16 control 66
 T8 and T16 common control functions 64



- T8/T16 control 67
- TC16H(D)07h 29
- TC16L(D)06h 30
- TC8 control 62
- TC8H(D)05h 30
- TC8L(D)04h 30
- voltage detection 68
- watch-dog timer 72
- register description
 - counter/timer2 ls-byte hold 30
 - counter/timer2 ms-byte hold 29
 - counter/timer8 control 30
 - counter/timer8 high hold 30
 - counter/timer8 low hold 30
 - CTR2 counter/timer 16 Control 34
 - CTR3 T8/T16 control 36
 - stop mode recovery2 37
 - T16_capture_LO 29
 - T8 and T16 common functions 32
 - T8_capture_HI 29
 - T8_capture_LO 29
- register file 27
 - expanded 23
- register pointer 26
 - detail 28
- reset pin function 22
- resets and WDT 61

S

- SCLK circuit 55
- single-pass mode
 - T16_OUT 44
 - T8_OUT 40
- stack 28
- standard test conditions 10
- standby modes 1
- stop instruction, counter/timer 51
- stop mode recovery
 - 2 register 58
 - source 56
- stop mode recovery 2 58
- stop mode recovery register 54

T

- T16 transmit mode 43
- T16_Capture_HI 29
- T8 transmit mode 37
- T8_Capture_HI 29
- test conditions, standard 10
- test load diagram 10
- timing diagram, AC 13
- transmit mode flowchart 38

V

- VCC 5
- voltage
 - brown-out/standby 61
 - detection and flags 62
- voltage detection register 68

W

- watch-dog timer
 - mode registerwatch-dog timer mode
 - register 59
 - time select 60

X

- XTAL1 5
- XTAL1 pin function 15
- XTAL2 5
- XTAL2 pin function 15

Z

- ZLP32300 family members 1