Preliminary

U62H1708

Automotive Fast 128K x 8 SRAM

Features

- ☐ 131072 x 8 bit static CMOS RAM
- ☐ 35 and 55 ns Access Time
- ☐ Common data inputs and data outputs
- ☐ Three-state outputs
- ☐ Typ. operating supply current
  - 35 ns: 45mA
  - 55 ns: 30mA
- ☐ Standby current <100µA at 125°C
- ☐ TTL/CMOS-compatible
- ☐ Power supply voltage 5 V
- ☐ Operating temperature range
  - -40 °C to 85 °C
  - -40 °C to 125 °C
- ☐ QS 9000 Quality Standard
- ☐ ESD protection > 2000 V (MIL STD 883C M3015.7)
- ☐ Latch-up immunity >100 mA
- ☐ Package: SOP32 (450 mil)
  - TSOP I 32
  - sTSOP I 32

Description

The U62H1708 is a static RAM manufactured using a CMOS process technology with the following operating modes:
- Read   - Standby
- Write   - Data Retention
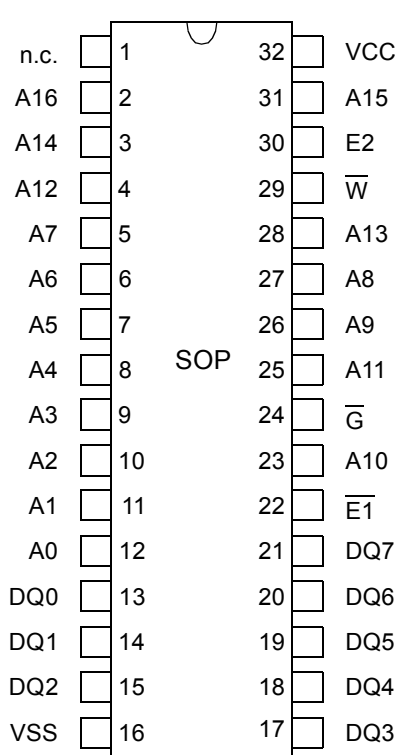
The memory array is based on a 6-Transistor cell.

The circuit is activated by the rising edge of E2 (at $\overline{E1}$ = L), or the falling edge of $\overline{E1}$ (at E2 = H). The address and control inputs open simultaneously. According to the information of $\overline{W}$ and $\overline{G}$, the data inputs, or outputs, are active. During the active state ($\overline{E1}$ = L and E2 = H) each address change leads to a new Read cycle. In a Read cycle, the data outputs are activated by the falling edge of $\overline{G}$, afterwards the data word will be available at the outputs DQ0-DQ7. After the address change, the data outputs go High-Z until the new information is available. The data outputs have no preferred state. If the memory is driven by CMOS levels in the active state, and if there is no change of the address, data input and control signals $\overline{W}$ or $\overline{G}$, the operating current (I_O = 0 mA) drops to the value of the operating current in the Standby mode. The Read cycle is finished by the falling edge of $\overline{E2}$ or $\overline{W}$, or by the rising edge of $\overline{E1}$, respectively.
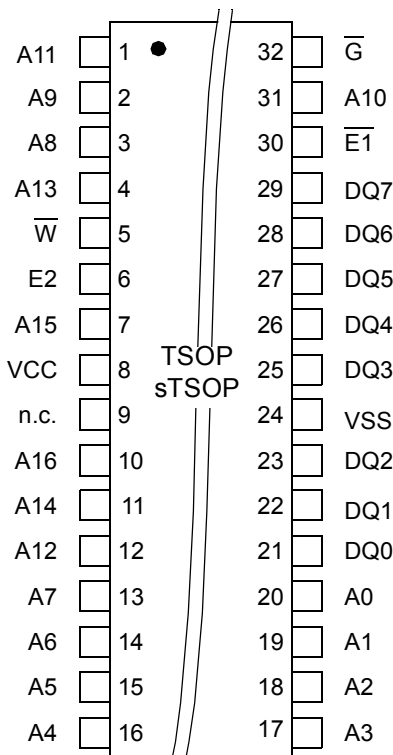
Data retention is guaranteed down to 2 V. With the exception of $\overline{E1}$ and E2, all inputs consist of NOR gates, so that no pull-up/pull-down resistors are required.

Pin Configuration

SOP — Top View

	SOP	
n.c.	1	VCC 32
A16	2	A15 31
A14	3	E2 30
A12	4	$\overline{W}$ 29
A7	5	A13 28
A6	6	A8 27
A5	7	A9 26
A4	8	A11 25
A3	9	$\overline{G}$ 24
A2	10	A10 23
A1	11	$\overline{E1}$ 22
A0	12	DQ7 21
DQ0	13	DQ6 20
DQ1	14	DQ5 19
DQ2	15	DQ4 18
VSS	16	DQ3 17

TSOP sTSOP — Top View

	TSOP sTSOP	
A11	1	$\overline{G}$ 32
A9	2	A10 31
A8	3	$\overline{E1}$ 30
A13	4	DQ7 29
$\overline{W}$	5	DQ6 28
E2	6	DQ5 27
A15	7	DQ4 26
VCC	8	DQ3 25
n.c.	9	VSS 24
A16	10	DQ2 23
A14	11	DQ1 22
A12	12	DQ0 21
A7	13	A0 20
A6	14	A1 19
A5	15	A2 18
A4	16	A3 17

Pin Description

Signal Name	Signal Description
A0 - A16	Address Inputs
DQ0 - DQ7	Data In/Out
$\overline{E1}$	Chip Enable 1
E2	Chip Enable 2
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
VCC	Power Supply Voltage
VSS	Ground
n.c.	not connected

ZMD

Block Diagram
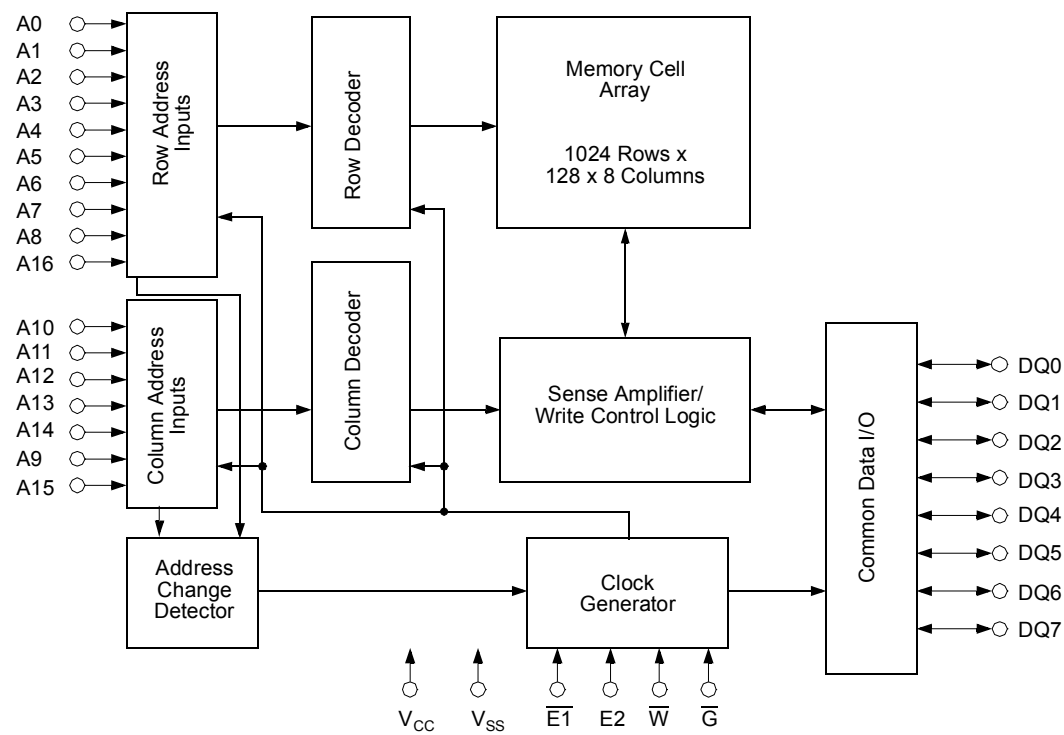
Truth Table

Operating Mode	$\overline{E1}$	E2	$\overline{W}$	$\overline{G}$	DQ0 - DQ7
Standby/not selected	*	L	*	*	High-Z
	H	*	*	*	High-Z
Internal Read	L	H	H	H	High-Z
Read	L	H	H	L	Data Outputs Low-Z
Write	L	H	L	*	Data Inputs High-Z

* H or L

Characteristics

All voltages are referenced to V_{SS} = 0 V (ground).
All characteristics are valid in the power supply voltage range and in the operating temperature range specified.
Dynamic measurements are based on a rise and fall time of $\leq$ 5 ns, measured between 10 % and 90 % of V_I, as well as
input levels of V_{IL} = 0 V and V_{IH} = 3 V. The timing reference level of all input and output signals is 1.5 V,
with the exception of the t_{dis}-times and t_{en}-times, in which cases transition is measured ±200 mV from steady-state voltage.

Absolute Maximum Ratings [a]		Symbol	Min.	Max.	Unit
Power Supply Voltage		V_{CC}	-0.5	7	V
Input Voltage		V_I	-0.5	V_{CC} + 0.5 [b]	V
Output Voltage		V_O	-0.5	V_{CC} + 0.5 [b]	V
Power Dissipation		P_D	-	1	W
Operating Temperature	K-Type	T_a	-40	85	°C
	A-Type		-40	125	
Storage Temperature		T_{stg}	-65	150	°C
Output Short-Circuit Current at V_{CC} = 5 V and V_O = 0 V [c]		$\lvert I_{OS} \rvert$		200	mA

[a] Stresses greater than those listed under „Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

[b] Maximum voltage is 7 V

[c] Not more than 1 output should be shorted at the same time. Duration of the short circuit should not exceed 30 s.

Recommended Operating Conditions	Symbol	Conditions	Min.	Max.	Unit
Power Supply Voltage	V_{CC}		4.5	5.5	V
Input Low Voltage*	V_{IL}		-0.3	0.8	V
Input High Voltage	V_{IH}		2.2	V_{CC} + 0.3	V

[d] -2 V at Pulse Width 10 ns

Electrical Characteristics	Symbol	Conditions		35		55		Unit
				Min.	Max.	Min.	Max.	
Supply Current - Operating Mode	$I_{CC(OP)}$	V_{CC} V_{IL} V_{IH} t_{cW} t_{cW} t_{cW}	= 5.5 V = 0.8 V = 2.2 V = 35 ns = 55 ns = 70 ns		50 35^{e} 30^{e}		- 35 30^{e}	mA mA mA
Supply Current - Standby Mode (CMOS level)	$I_{CC(SB)}$	V_{CC} $V_{\overline{E1}}= V_{E2}$	= 5.5 V $= V_{CC} - 0.2$ V		100		100	µA
Supply Current - Standby Mode (TTL level)	$I_{CC(SB)1}$	V_{CC} $V_{\overline{E1}}= V_{E2}$ K-Type A-Type	= 5.5 V = 2.2 V		10 20		10 20	mA mA
Output High Voltage	V_{OH}	V_{CC} I_{OH}	= 4.5 V = -4.0 mA	2.4		2.4		V
Output Low Voltage	V_{OL}	V_{CC} I_{OL}	= 4.5 V = 8.0 mA		0.4		0.4	V
Input High Leakage Current	I_{IH}	V_{CC} V_{IH}	= 5.5 V = 5.5 V		2		2	µA
Input Low Leakage Current	I_{IL}	V_{CC} V_{IL}	= 5.5 V = 0 V	-2		-2		µA
Output High Current	I_{OH}	V_{CC} V_{OH}	= 4.5 V = 2.4 V		-4		-4	mA
Output Low Current	I_{OL}	V_{CC} V_{OL}	= 4.5 V = 0.4 V	8		8		mA
Output Leakage Current High at Three-State Outputs	I_{OHZ}	V_{CC} V_{OH}	= 5.5 V = 5.5 V		2		2	µA
Low at Three-State Outputs	I_{OLZ}	V_{CC} V_{OL}	= 5.5 V = 0 V	-2		-2		µA

[e] This parameter is guaranteed, but not tested.

Switching Characteristics Read Cycle	Symbol		35		55		Unit
	Alt.	IEC	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	t_{cR}	35		55		ns
Address Access Time to Data Valid	t_{AA}	$t_{a(A)}$		35		55	ns
Chip Enable Access Time to Data Valid	t_{ACE}	$t_{a(E)}$		35		55	ns
$\overline{G}$ LOW to Data Valid	t_{OE}	$t_{a(G)}$		15		25	ns
$\overline{E1}$ HIGH or E2 LOW to Output in High-Z	t_{HZCE}	$t_{dis(E)}$		12		15	ns
$\overline{G}$ HIGH to Output in High-Z	t_{HZOE}	$t_{dis(G)}$		12		15	ns
$\overline{E1}$ LOW or E2 HIGH to Output in Low-Z	t_{LZCE}	$t_{en(E)}$	5		5		ns
$\overline{G}$ LOW to Output in Low-Z	t_{LZOE}	$t_{en(G)}$	0		0		ns
Output Hold Time from Address Change	t_{OH}	$t_{v(A)}$	5		5		ns
$\overline{E1}$ LOW or E2 HIGH to Power-Up Time	t_{PU}		0		0		ns
$\overline{E1}$ HIGH or E2 LOW to Power-Down Time	t_{PD}			35		55	ns

Switching Characteristics Write Cycle	Symbol		35		55		Unit
	Alt.	IEC	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	t_{cW}	35		55		ns
Write Pulse Width	t_{WP}	$t_{w(W)}$	20		35		ns
Write Setup Time	t_{WP}	$t_{su(W)}$	20		35		ns
Address Setup Time	t_{AS}	$t_{su(A)}$	0		0		ns
Address Valid to End of Write	t_{AW}	$t_{su(A-WH)}$	20		35		ns
Chip Enable Setup Time	t_{CW}	$t_{su(E)}$	25		40		ns
Pulse Width Chip Enable to End of Write	t_{CW}	$t_{w(E)}$	25		40		ns
Data Setup Time	t_{DS}	$t_{su(D)}$	15		25		ns
Data Hold Time	t_{DH}	$t_{h(D)}$	0		0		ns
Address Hold from End of Write	t_{AH}	$t_{h(A)}$	0		0		ns
$\overline{W}$ LOW to Output in High-Z	t_{HZWE}	$t_{dis(W)}$		15		20	ns
$\overline{G}$ HIGH to Output in High-Z	t_{HZOE}	$t_{dis(G)}$		12		15	ns
$\overline{W}$ HIGH to Output in Low-Z	t_{LZWE}	$t_{en(W)}$	0		0		ns
$\overline{G}$ LOW to Output in Low-Z	t_{LZOE}	$t_{en(G)}$	0		0		ns

Data Retention Mode

Data Retention Characteristics	Symbol		Conditions	Min.	Typ.	Max.	Unit
	Alt.	IEC					
Data Retention Supply Voltage		$V_{CC(DR)}$		2		5.5	V
Data Retention Supply Current		$I_{CC(DR)}$	$V_{CC(DR)} = 3$ V $V_{\overline{E1}} = V_{E2} = V_{CC(DR)} - 0.2$ V			60	μA
Data Retention Setup Time	t_{CDR}	$t_{su(DR)}$	See Data Retention Waveforms (below)	0			ns
Operating Recovery Time	t_R	t_{rec}		t_{cR}			ns

Data Retention Mode $\overline{E1}$ - controlled
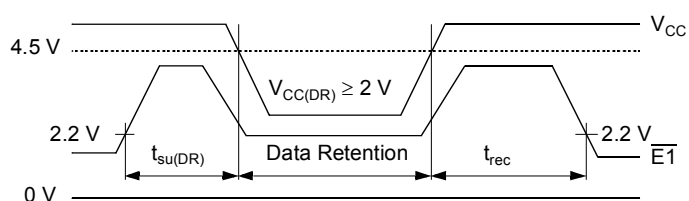
$V_{E2(DR)} \geq V_{CC(DR)} - 0.2$ V or $V_{E2(DR)} \leq 0.2$ V
$V_{CC(DR)} - 0.2$ V $\leq V_{\overline{E1}(DR)} \leq V_{CC(DR)} + 0.3$ V

Data Retention Mode E2 - controlled
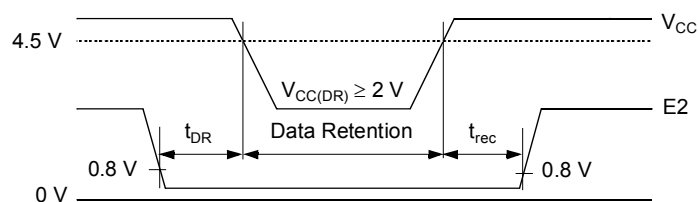
$V_{E1(DR)} \geq V_{CC(DR)} - 0.2$ V or $V_{E1(DR)} \leq 0.2$ V
$V_{E2(DR)} \leq 0.2$ V

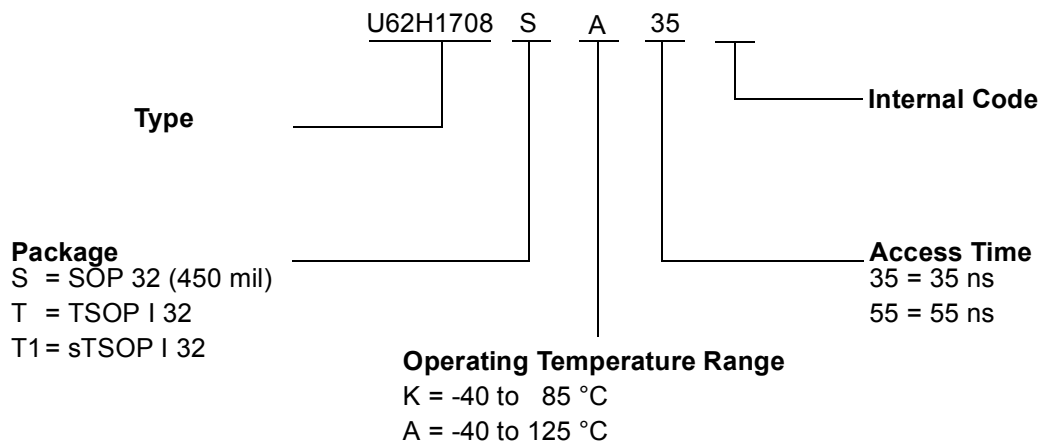**Test Configuration for Functional Check**
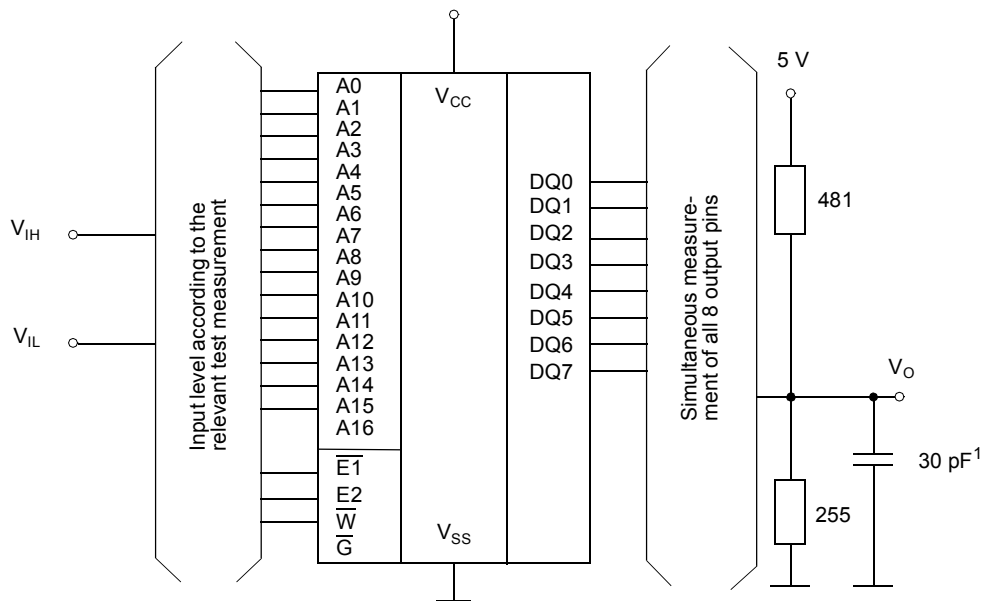
[1] In measurement of $t_{dis(E)}$, $t_{dis(W)}$, $t_{en(E)}$, $t_{en(W)}$, $t_{en(G)}$ the capacitance is 5 pF.

Capacitance	Conditions		Symbol	Min.	Max.	Unit
Input Capacitance	V_{CC} V_I	= 5.0 V = V_{SS}	C_I		7	pF
Output Capacitance	f T_a	= 1 MHz = 25 °C	C_o		7	pF

All pins not under test must be connected with ground by capacitors.

IC Code Numbers

U62H1708   S   A   35

Type

Internal Code

Package
S = SOP 32 (450 mil)
T = TSOP I 32
T1 = sTSOP I 32

Access Time
35 = 35 ns
55 = 55 ns

Operating Temperature Range
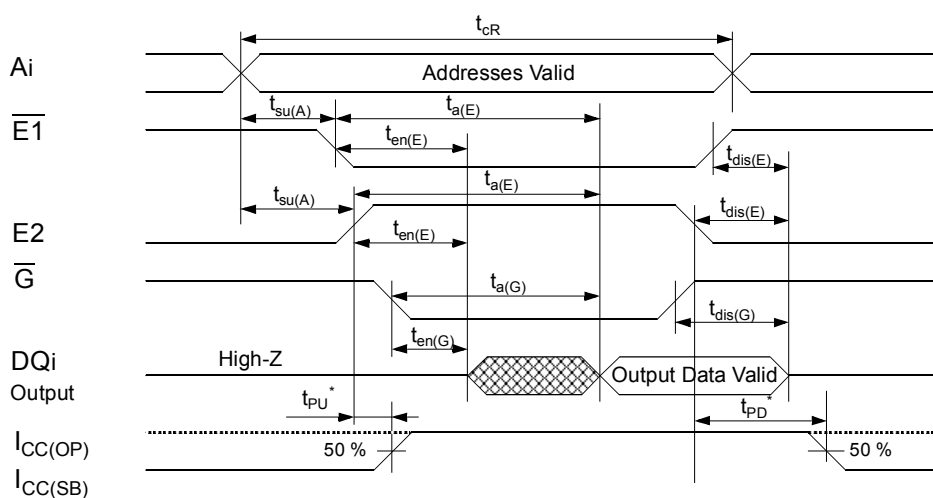K = -40 to   85 °C
A = -40 to 125 °C

The date of manufacture is given by the last 4 digits of the third line of the mark, the first 2 digits indicating the year, and the last 2 digits the calendar week.
Assembly location and trace code are shown in line 4.

Read Cycle 1: A$_i$-controlled (during Read Cycle : $\overline{E1} = \overline{G} = V_{IL}$, $\overline{W} = E2 = V_{IH}$)

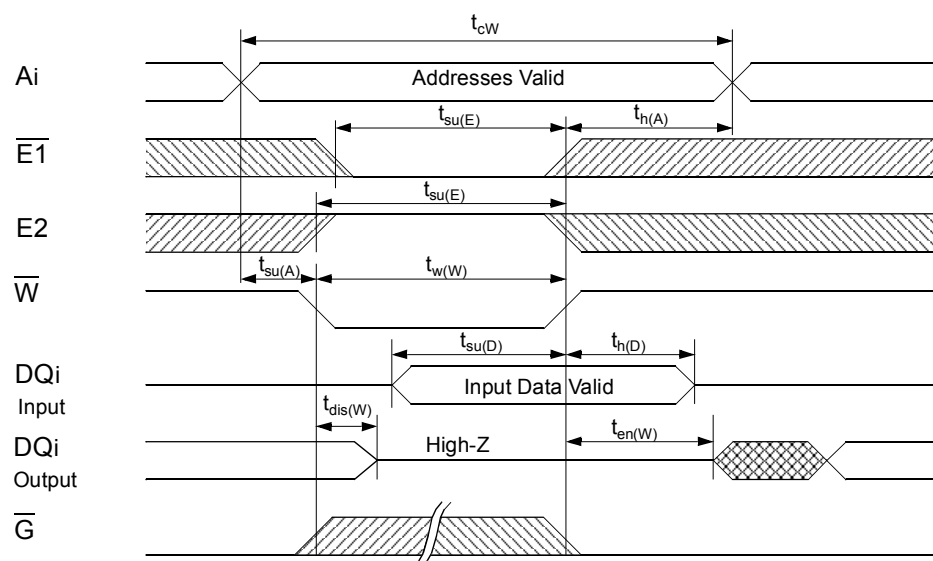Ai — Address Valid — t_{cR}

DQi Output — Previous Data Valid — Output Data Valid — $t_{a(A)}$, $t_{v(A)}$
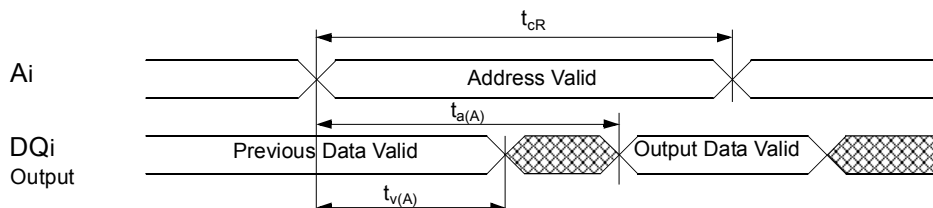
Read Cycle 2: $\overline{G}$-, $\overline{E1}$, E2-controlled (during Read Cycle: $\overline{W} = V_{IH}$)

Ai — Addresses Valid — t_{cR}

$\overline{E1}$ — $t_{su(A)}$, $t_{en(E)}$, $t_{a(E)}$, $t_{dis(E)}$

E2 — $t_{su(A)}$, $t_{en(E)}$, $t_{a(E)}$, $t_{dis(E)}$

$\overline{G}$ — $t_{a(G)}$, $t_{en(G)}$, $t_{dis(G)}$

DQi Output — High-Z — Output Data Valid

$I_{CC(OP)}$ / $I_{CC(SB)}$ — t_{PU}*, 50 %, t_{PD}*, 50 %

* The same applies to $\overline{E1}$

Write Cycle1: $\overline{W}$-controlled

Ai — Addresses Valid — t_{cW}

$\overline{E1}$ — $t_{su(E)}$, $t_{h(A)}$

E2 — $t_{su(E)}$

$\overline{W}$ — $t_{su(A)}$, $t_{w(W)}$

DQi Input — Input Data Valid — $t_{su(D)}$, $t_{h(D)}$

DQi Output — $t_{dis(W)}$ — High-Z — $t_{en(W)}$
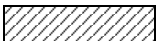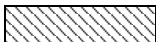
$\overline{G}$

Write Cycle 2: $\overline{E1}$-controlled
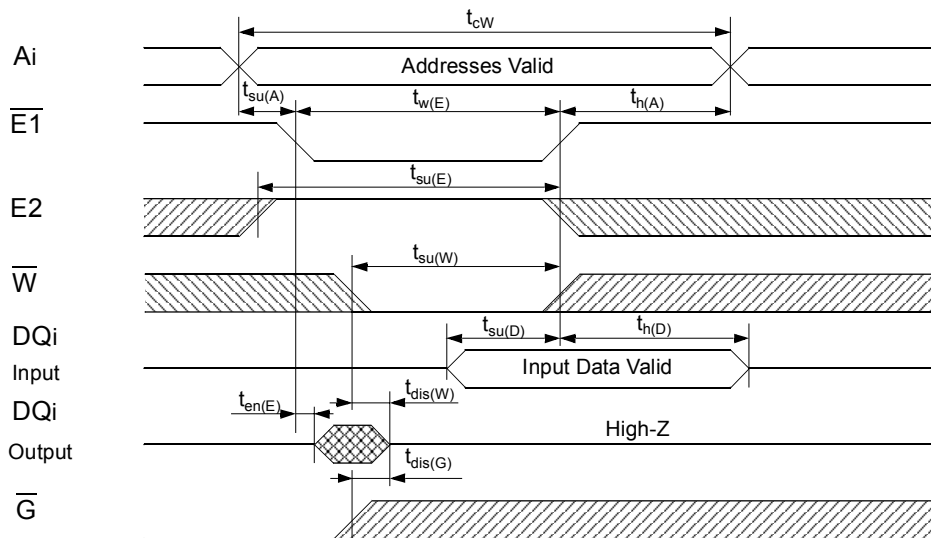
Write Cycle 3 (E2-controlled)
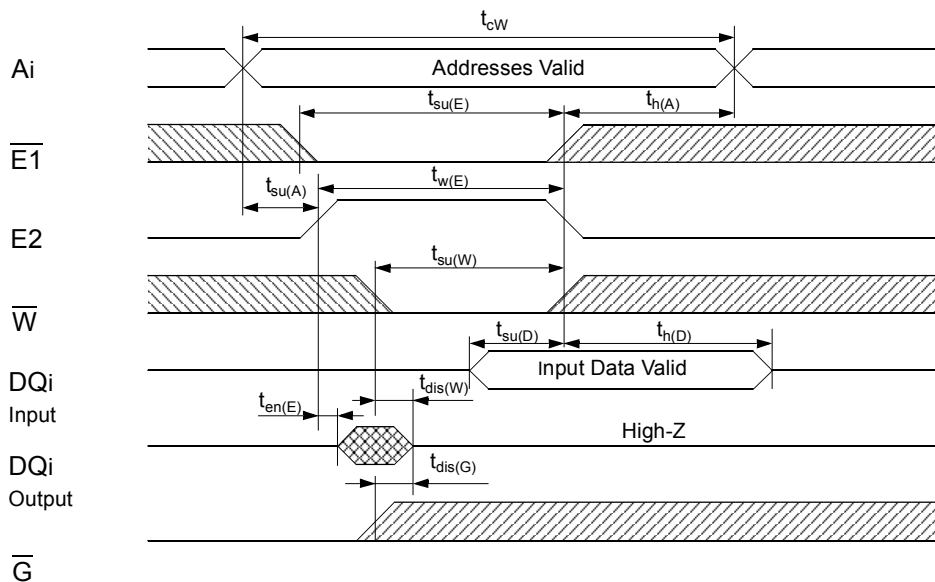
undefined · L- to H-level · H- to L-level

The information describes the type of component and shall not be considered as assured characteristics. Terms of delivery and rights to change design reserved.

LIFE SUPPORT POLICY

ZMD products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the ZMD product could create a situation where personal injury or death may occur.
Components used in life-support devices or systems must be expressly authorized by ZMD for such purpose.

LIMITED WARRANTY

The information in this document has been carefully checked and is believed to be reliable. However Zentrum Mikroelektronik Dresden AG (ZMD) makes no guarantee or warranty concerning the accuracy of said information and shall not be responsible for any loss or damage of whatever nature resulting from the use of, or reliance upon it. The information in this document describes the type of component and shall not be considered as assured characteristics.
ZMD does not guarantee that the use of any information contained herein will not infringe upon the patent, trademark, copyright, mask work right or other rights of third parties, and no patent or licence is implied hereby. This document does not in any way extent ZMD's warranty on any product beyond that set forth in its standard terms and conditions of sale.
ZMD reserves terms of delivery and reserves the right to make changes in the products or specifications, or both, presented in this publication at any time and without notice.