

## Quad 8 Bit DAC DIGITRIM

## Features

- ❑ 2.7 - 5.5V Power Supply
- ❑ Rail to Rail Input and Output Voltage Range
- ❑ Serial Three-Wire Interface
- ❑ Software Shutdown
- ❑ Simultaneous Update
- ❑ Internal PON with Clear
- ❑ Asynchronous Clear Input
- ❑ Serial Data Output
- ❑ 16 Pin QSOP Package
- ❑ Footprint Compatible to MAXIM's MAX534/533

## Applications

- ❑ Digital Offset and Amplification Adjustment
- ❑ MPU controlled Trimming Operations
- ❑ Usage for General Voltage Trimming Devices

## General Description

The DIGITRIM contains quad DAC channels with identical structure. There is an input register followed by a DAC register, resistor string DAC with externally supplied reference and a rail-to-rail voltage output buffer.

Using the three wire interface, data is clocked serial into the 12 bit shift register. Independent from the four addressing and command bits the contents of shift register is transferred to input register or DAC register when /LDAC goes low or a software command occurs. For daisy chaining applications incoming data is outputted delayed 12 or 12 ½ SCLK - clocks at DOUT.

After power on or hardware clear all registers are set to zero. The DIGITRIM circuits are manufactured using a 0.8-micron CMOS process.

## Functional Diagram

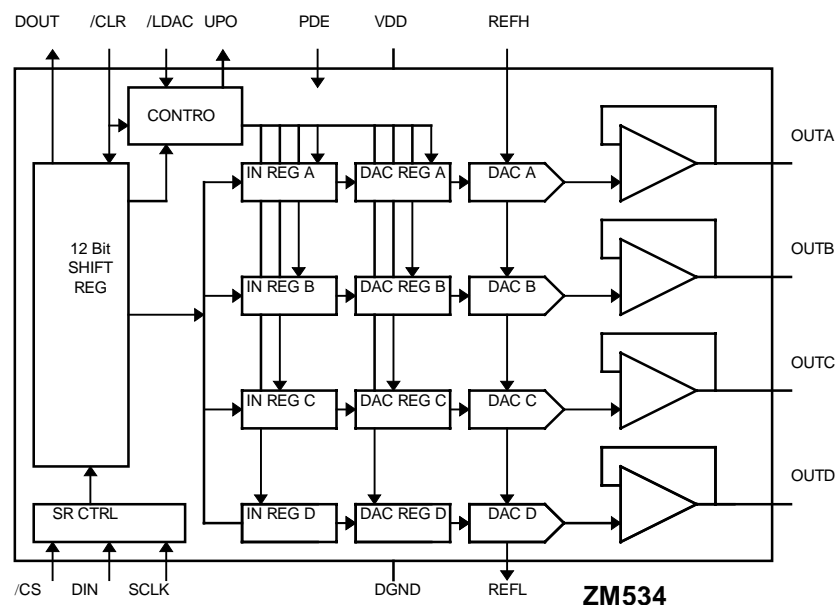


Figure 1. Block Diagram

## Pin Configuration

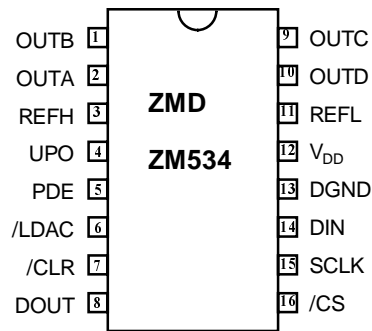


Figure2. Pin Configuration

## Pin Description

Name	Description	Name	Description
OUTB	DAC B Output	OUTC	DAC C Output
OUTA	DAC A Output	OUTD	DAC D Output
REFH	Reference Voltage Input (High)	REFL	Reference Voltage Input (Low)
UPO	User - Programmable Logic Output	VDD	Power Supply
PDE	Power Down Enable	GND	Ground
/LDAC	Load DAC register with the contents of the input register	DIN	Serial Data Input
/CLR	Clear DAC Input	SCLK	Serial Clock Input
/DOUT	Serial Data Output	/CS	Chip-Select Input

## Operating Characteristics

### Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device as indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply voltage $V_{DD}$ to GND	$V_{DD}$	-0.3		+7	V
Digital Input Voltage to GND	$V_I$	-0.3		$V_{DD}+0.3$	V
Digital Output Voltage to GND		-0.3		$V_{DD}+0.3$	V
REFH/REFL Input Voltage		-0.3		$V_{DD}+0.3$	V
OUTx Voltage		-0.3		$V_{DD}$	V
Maximum Current into Any Pin				50	mA
Continuous Power Dissipation (TA= + 70 °C) QSOP16	P			500	mW
Operating Temperature Range	T	-45		+85	°C
Storage Temperature Range	T <sub>stg</sub>	-55		+125	°C

## Electrical Characteristics

( $V_{DD}=+2,7$  to  $+5.5V$ ,  $V_{REFH}=4V$ ,  $REFL=GND=0V$ ,  $R_L=10k\Omega$ ,  $C_L=100pF$ ,  $T_A=T_{MIN}$  to  $T_{MAX}$ , Typical values are at  $V_{DD}=+5V$  and  $T_A=+25^\circ C$ )

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>Static Accuracy</b>						
Resolution					8	Bits
Integral Nonlinearity	INL	(Note1)			$\pm 1$	LSB
Differential Nonlinearity	DNL	Garanteed monotonic (all codes) (Note 1)			$\pm 1$	LSB
Zero-Code Error		Code=00 hex			$\pm 20$	mV
Zero-Code-Error Supply Rejection		Code=00 hex, $V_{DD}=4.5$ to $5.5V$			1	LSB
Zero Code Temperatur Coefficient		Code=00 hex		$\pm 10$		$\mu V/^\circ C$
Full Scale Error		Code=FF hex			$\pm 20$	mV
Full-Scale Error Supply Rejection		Code=FF hex			1	LSB
Full-Scale Temperature Coefficient		Code=FF hex		$\pm 10$		$\mu V/^\circ C$
<b>Reference Inputs</b>						
Input Voltage Range			0		$V_{DD}$	V
Input Resistance				85		$k\Omega$
Input Capacitance				10		pF
Channel-to-Channel Isolation		(Note 2)		-60		dB
AC Feedthrough		(Note 3)		-60		dB
<b>DAC Outputs</b>						
Output Voltage Range		$R_L=open$	0		$V_{REFH}$	V
Load Regulation		Code=FF hex, $R_L$ from $10k\Omega$ to $\infty$			0.25	LSB/mA
<b>Digital Inputs</b>						
Input High Voltage	$V_{IH}$		$0.7V_{DD}$			V
Input Low Voltage	$V_{IL}$				$0.3V_{DD}$	V
Input Current	$I_{IN}$	$V_{IN}=0V$ or $V_{DD}$			$\pm 1.0$	$\mu A$
Input Capacitance	$C_{IN}$	(Note 4)			10	pF
<b>Digital Outputs</b>						
Output High Voltage	$V_{OH}$	$I_{SOURCE}=0.1mA$	$V_{DD}-0.5$			V
Output Low Voltage	$V_{OL}$	$I_{SINK}=2mA$			0.4	V
<b>Dynamic Performance</b>						
Voltage-Output Slew Rate		Code=FF hex		0.8		V/ $\mu s$
Output Settling Time		To $\frac{1}{2}$ LSB, from code 00 to code FF hex (Note 5)		7		$\mu s$
Digital Feedthrough and Crosstalk		$V_{REFH}=0V$ , code 00 to FF hex (Note 6)		4		nV-s
Digital-to Analog Glitch Impulse		Code 80 hex to code 7F hex		45		nV-s
Signal-to-Noise Plus Distorsion Ratio	SINAD	$V_{REFH}=4V_{p-p}$ , at 1kHz, code=FF hex/ $V_{REFH}=4V_{p-p}$ , at 10kHz		80/70		dB
Multiplying Bandwidth		$V_{REFH}=0.5V_{p-p}$ , 3dB bandwitdh		500		kHz
Wideband Amplifier Noise				60		$\mu V_{RMS}$
<b>Power Supplies</b>						
Power-Supply Voltage	$V_{DD}$		2,7		5.5	V
Supply Current	$I_{DD}$			1,3		mA
Shutdown Current				2.5	10	$\mu A$

## Timing Characteristics

( $V_{DD}=+4.5$  to  $+5.5V$ ,  $V_{REFH}=4V$ ,  $REFL=GND=0V$ ,  $C_L=100pF$ ,  $T_A=T_{MIN}$  to  $T_{MAX}$ , Typical values are at  $V_{DD}=+5V$  and  $T_A=+25^{\circ}C$ )

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
$V_{DD}$ Rise to /CS Fall Setup Time	$t_{DSC}$				50	$\mu s$
/LDAC Pulse Width Low	$t_{LDAC}$		40	20		ns
/CS Rise to /LDAC Fall Setup Time	$t_{CLI}$		40			ns
/CLR Pulse Width Low	$t_{CLW}$		40	20		ns
/CS Pulse Width High	$t_{CSW}$		90			ns
<b>Serial Interface Timing</b>						
SCLK Clock Frequency (Note 8)	$f_{CLK}$				10	MHz
SCLK Pulse Width High	$t_{CH}$		40			ns
SCLK Pulse Width Low	$t_{CL}$		40			ns
/CS Fall to SCLK Rise Setup Time	$t_{CSS}$		40			ns
SCLK Rise to /CS Rise Hold Time	$t_{CSH}$		0			ns
DIN to SCLK Rise to Setup Time	$t_{DS}$		40			ns
DIN to SCLK Rise to Hold Time	$t_{DH}$		0			ns
SCLK Rise to DOUT Valid propagation Delay Time (Note 9)	$t_{DO1}$				200	ns
SCLK Fall to DOUT Valid propagation Delay Time (Note 10)	$t_{DO2}$				210	ns
SCLK Rise to /CS Fall Delay	$t_{CS0}$		40			ns
/CS Rise to SCLK Rise Setup Time	$t_{CS1}$		40			ns

Note 1: INL and DNL are measured with  $R_L$  referenced to Ground. Nonlinearity is measured from the first code that is greater than or equal to the maximum offset specification to the code FF hex (full scale).

Note 2:  $V_{REFH} = 4V_{p-p}$ , 10kHz. Channel to-channel isolation is measured by setting one DAC's code to FF hex and setting all other DAC's codes to 00H.

Note 3:  $V_{REFH} = 4V_{p-p}$ , 10kHz. DAC code = 00 hex.

Note 4: Guaranteed by design not production tested.

Note 5: Output settling time is measured from 50% point of the rising edge of /CS to  $\frac{1}{2}$  LSB of VOUT's final value.

Note 6: Digital crosstalk is defined as the glitch energy at any DAC output in response to a full-scale step change on any other. DAC

Note 7: If /LDAC is activated prior to /CS rising edge, it must stay low for  $t_{LDAC}$  or longer after /CS goes high.

Note 8: When DOUT is not used. If DOUT is used,  $f_{SCLK}$  max is 4 MHz, due to DOUT propagation delay.

Note 9: Serial data clocked out at SCLK's rising edge (measured from 50% of the clock edge to 20% or 80% of  $V_{DD}$ )

Note 10: Serial data clocked out at SCLK's falling edge (measured from 50% of the clock edge to 20% or 80% of  $V_{DD}$ )

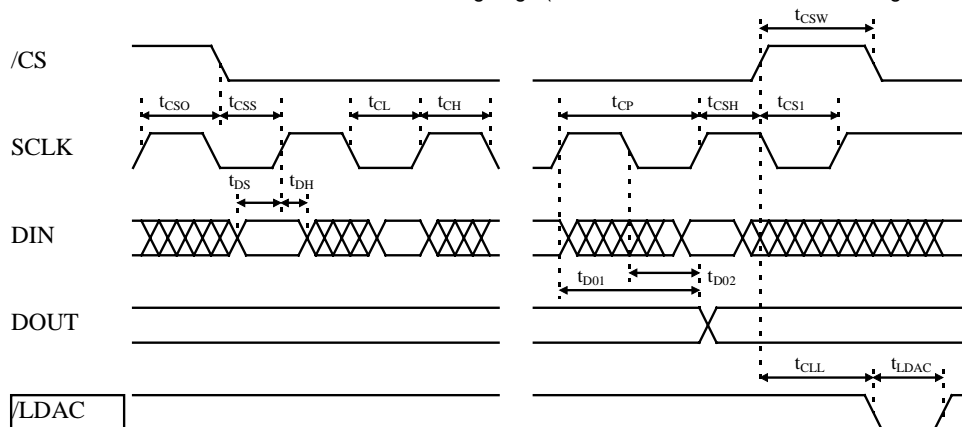


Figure 3. Serial-Interface Timing Diagram

## Programming the DIGITRIM

To program the DIGITRIM a serial bit stream is provided to input DIN.

The DIN data bits are clocked in a 12 Bit shift register with rising edge of SCLK. while /CS=Low  
That means, only the last 12 Bits are important.

Data can be transfered in blocks. Between the blocks SCLK should remaining on low level.

With the raising edge of /CS data will be clocked into input register and commands will be executed.

### Serial Data Format

first bits								last bits			
A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
Adress and Control Bits				Data Bits							

### Serial-Interface Programming Commands

A1	A0	C1	C0	D7..D0	/LDAC	Function
<b>Load Input Register</b>						
0	0	0	1	8-bit DAC data	1	Load Input Register A, outputs unchanged
0	1	0	1	8-bit DAC data	1	Load Input Register B, outputs unchanged
1	0	0	1	8-bit DAC data	1	Load Input Register C, outputs unchanged
1	1	0	1	8-bit DAC data	1	Load Input Register D, outputs unchanged
<b>Load Input Register and update all DAC-Registers on /CS rising edge</b>						
0	0	1	1	8-bit DAC data	1	Load Input Register A, outputs updated
0	1	1	1	8-bit DAC data	1	Load Input Register B, outputs updated
1	0	1	1	8-bit DAC data	1	Load Input Register C, outputs updated
1	1	1	1	8-bit DAC data	1	Load Input Register D, outputs updated
<b>Software /LDAC, update all DAC registers with input register data on /CS rising edge, leave shutdown</b>						
0	1	0	0	XXXXXXXX	1	Update all DAC registers with input register data
<b>Load all DAC register with the shift register data</b>						
1	0	0	0	8-bit DAC data	X	Update all DAC outputs with the serial data
<b>Software Shutdown for all buffer amplifier, contents of register remains</b>						
1	1	0	0	XXXXXXXX	X	Reduces power consumption rapidly
<b>User-Programmable Output programming</b>						
0	0	1	0	XXXXXXXX	X	UPO goes LOW
0	1	1	0	XXXXXXXX	X	UPO goes High
<b>No operation</b>						
0	0	0	0	XXXXXXXX	X	Allows to shift data throught IC without effect in daisy chaining applications
<b>SET DOUT Phase, update all DAC registers</b>						
1	1	1	0	XXXXXXXX	X	DOUT data valid at SCLK rising, Mode 1)
1	0	1	0	XXXXXXXX	X	DOUT data valid at SCLK falling, Mode 0 default)

## Special Pins and Functions

Output UPO	Level is user-programmable by software command Can be applied for wide user defined control purposes..
Input PDE:	If high, the software power down is enabled
Input /CLR	Clears all input and DAC registers to zero.
Input /CS	Enables the programming with SCLK and DIN The rising edge of /CS starts the execution of received commands. No effect for /LDAC, /CLR, PDE !
Input /LDAC	Updates the contents of DAC registers from input registers. If /LDAC=Low all DAC registers are transparent
Output DOUT	Shift register non three-state output for daisy chaining applications. Software programmable 12 or 12 ½ clock delay to data in clock SCLK. If Data valid at rising edge of DOUT then delay 12 clocks to SCLK clock or if Data valid at falling edge of DOUT then delay 12 ½ clocks to DIN

## Output Voltage in dependence of Reference Voltage and Programming Code

The unipolar output voltage of 8 Bit DACs is

$$V_{OUT} = (\text{bin-to-dec converted Code} * V_{REFH}) / 256.$$

The input resistance of resistor string is independent from code typical 85kΩ.

DAC register Contents		Analog Output
MSB	LSB	
1111	1111	$+V_{REFH} * (255/256)$
1000	0001	$+V_{REFH} * (129/256)$
1000	0000	$+V_{REFH} * (128/256)$
0111	1111	$+V_{REFH} * (127/256)$
0000	0001	$+V_{REFH} * (1/256)$
0000	0000	0V

## Diagrams

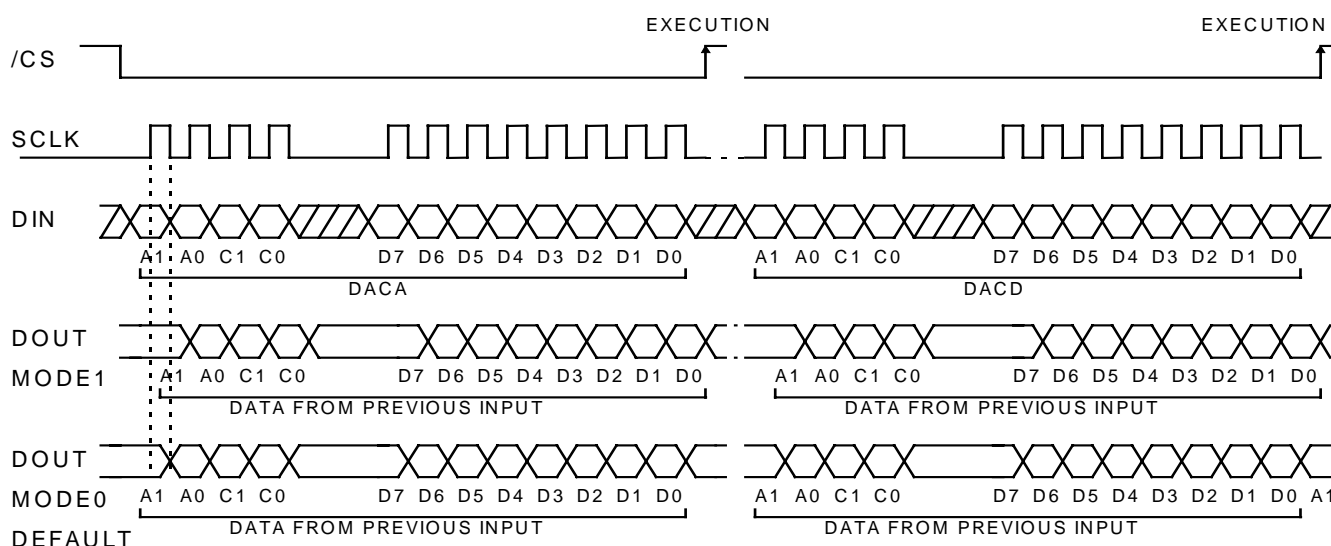


Figure4. 3-Wire Interface Timing

## Notes for Application

Often it is necessary to use more than one DIGITRIM in one device.

Figure 5. shows the daisy-chaining of three DIGITRIMS.

The Three-Wire interface commonly uses the inputs SCLK, DIN, /CS.

The DOUT provides the next DIN. After 36 rising edges of SCLK the complete programming information is clocked in. Simultaneous output can take place for example by sending the Software /LDAC Command.

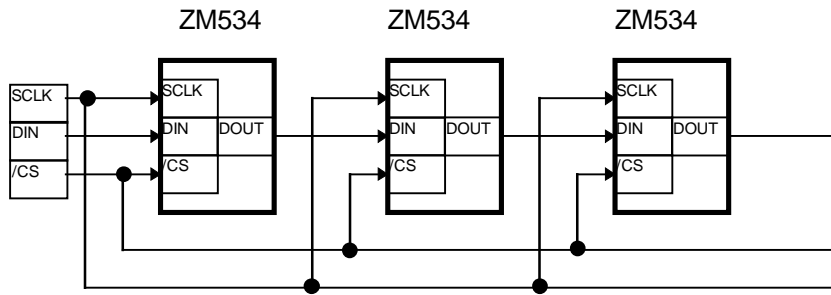


Figure 5. Daisy-chaining application

Figure 6. shows the common use of DIN and separately control of /CS.

To simultaneous update DAC registers use /LDAC.

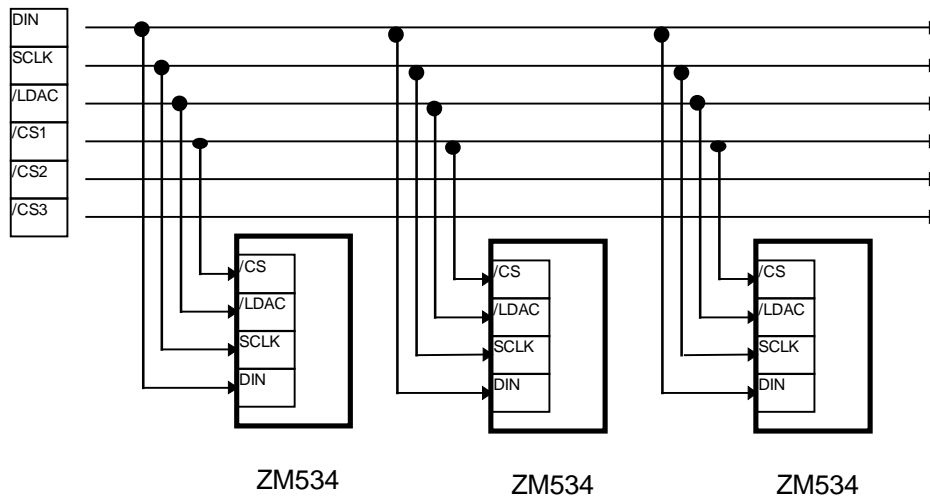


Figure 6. Application with common DIN and selection by /CS

## Basic Application

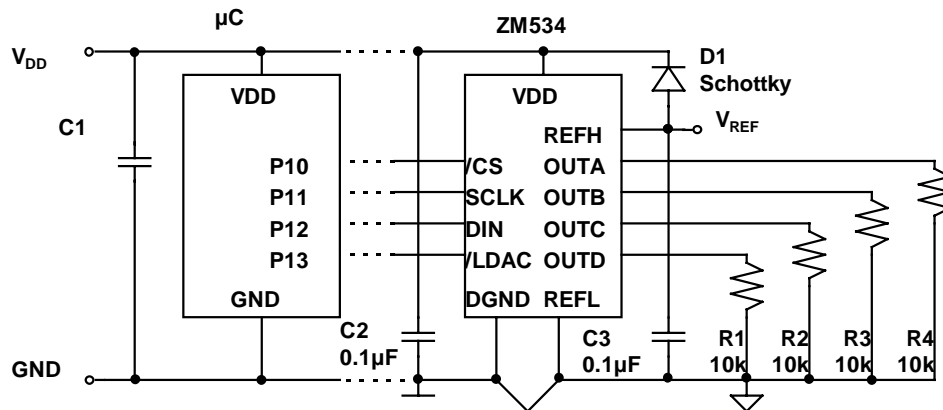


Figure 7. Basic Application

The voltage on REFH or REFL should never exceed  $V_{DD}$ , when not guaranteed, insert schottky diode to  $V_{DD}$ !  
 Do not apply signals to logic inputs during power off !  
 In all applications  $V_{DD}$  had to be bypassed to DGND with a  $0.1\mu F$  capacitor.

The information describes the type of component and shall not be considered as assured characteristic. Terms of delivery and rights to change design reserved.

### Zentrum Mikroelektronik Dresden GmbH

Grenzstraße 28 • D-01109 Dresden • Germany • P.O.B 80 01 34 • D-01101 Dresden • Germany  
 Phone: +49 351 88 22 306 • Fax +49 351 88 22 337 • Email: sales@zmd.de • <http://www.zmd.de>