

54F/74F132 Quad 2-Input NAND Schmitt Trigger

General Description

The 'F132 contains four 2-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional NAND gates.

Each circuit contains a 2-input Schmitt trigger followed by level shifting circuitry and a standard FAST® output structure. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input

threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800 mV) is determined by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

Features

- Guaranteed 4000V minimum ESD protection
- Standard Military Drawing (SMD)
- 5962-89487

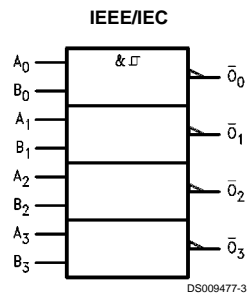
Ordering Code: See Section 0

Commercial	Military	Package Number	Package Description
74F132PC		N14A	14-Lead (0.300" Wide) Molded Dual-In-Line
	54F132DM (Note 2)	J14A	14-Lead Ceramic Dual-In-Line
74F132SC (Note 1)		M14A	14-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F132SJ (Note 1)		M14D	14-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F132FM (Note 2)	W14B	14-Lead Cerpack
	54F132LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

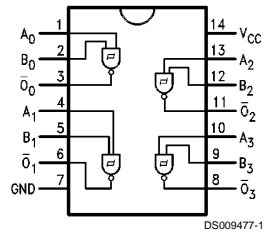
Logic Symbol



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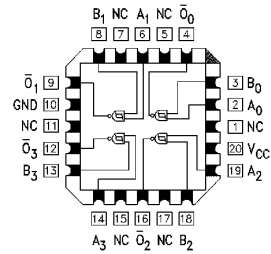
Connection Diagrams

Pin Assignment for
DIP, SOIC and Flatpak



DS009477-1

Pin Assignment
for LCC



DS009477-2

Unit Loading/Fan Out See Section 0 for U.L. definitions

Pin Names	Description	54F74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_n, B_n	Inputs	1.0/1.0	20 μ A/-0.6 mA
\bar{O}_n	Outputs	50/33.3	-1 mA/20 mA

DSXXXX

Function Table

Inputs		Outputs
A	B	\bar{O}
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 4)	-0.5V to +7.0V
Input Current (Note 4)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
TRI-STATE® Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

Note 3: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 4: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{T+}	Positive-going Threshold	1.5		2.0	V	5.0	
V _{T-}	Negative-going Threshold	0.7		1.1	V	5.0	
ΔV _T	Hysteresis (V _{T+} - V _{T-})	0.4			V	5.0	
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC}	2.5		V	Min	I _{OH} = -1 mA
		74F 10% V _{CC}	2.5				
		74F 5% V _{CC}	2.7				
V _{OL}	Output LOW Voltage	54F 10% V _{CC}		0.5	V	Min	I _{OL} = 20 mA
		74F 10% V _{CC}		0.5			
I _{IH}	Input HIGH Current	54F		20.0	μA	Max	V _{IN} = 2.7V
		74F		5.0			
I _{BVI}	Input HIGH Current Breakdown Test	54F		100	μA	Max	V _{IN} = 7.0V
		74F		7.0			
I _{CEX}	Output HIGH Leakage Current	54F		250	μA	Max	V _{OUT} = V _{CC}
		74F		50			
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F		3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6	mA	Max	V _{IN} = 0.5V
I _{OS}	Output Short-Circuit Current		-60	-150	mA	Max	V _{OUT} = 0V
I _{CCH}	Power Supply Current			17.0	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current			18.0	mA	Max	V _O = LOW

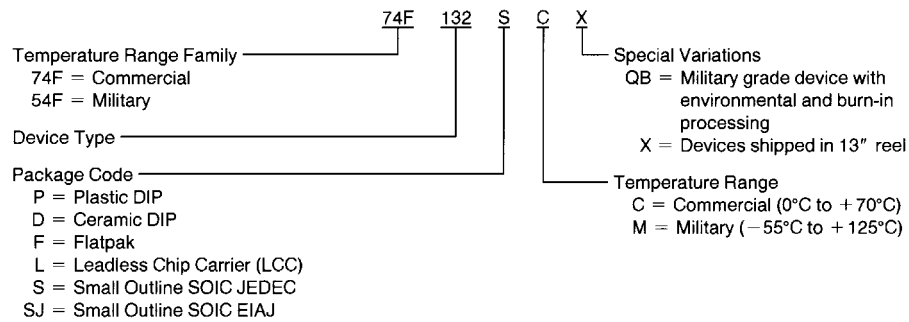
AC Electrical Characteristics

See Section 0 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Mil C _L = 50 pF		T _A , V _{CC} = Com C _L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t _{PLH}	Propagation Delay	4.0		10.5	2.0	13.0	3.5	12.0	ns	◆◆◆◆
t _{PHL}	A _n , B _n to \bar{O}_n	5.0		12.5	4.5	16.0	5.0	13.0		

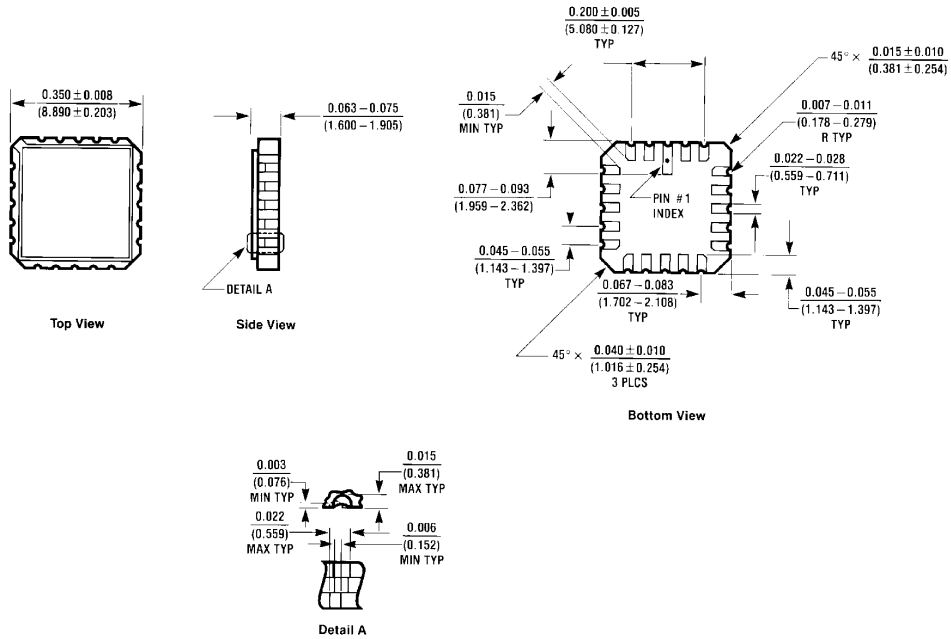
Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



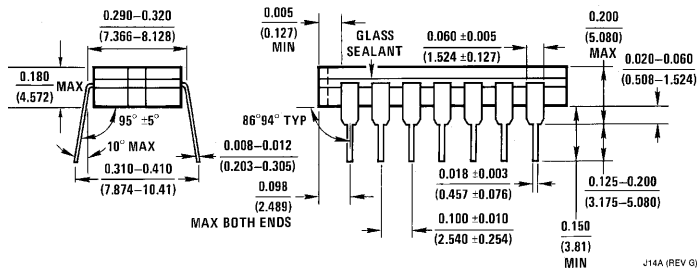
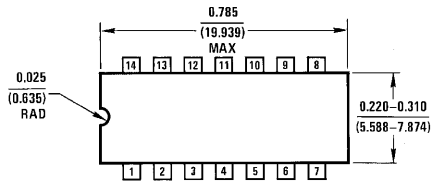
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Physical Dimensions inches (millimeters) unless otherwise noted



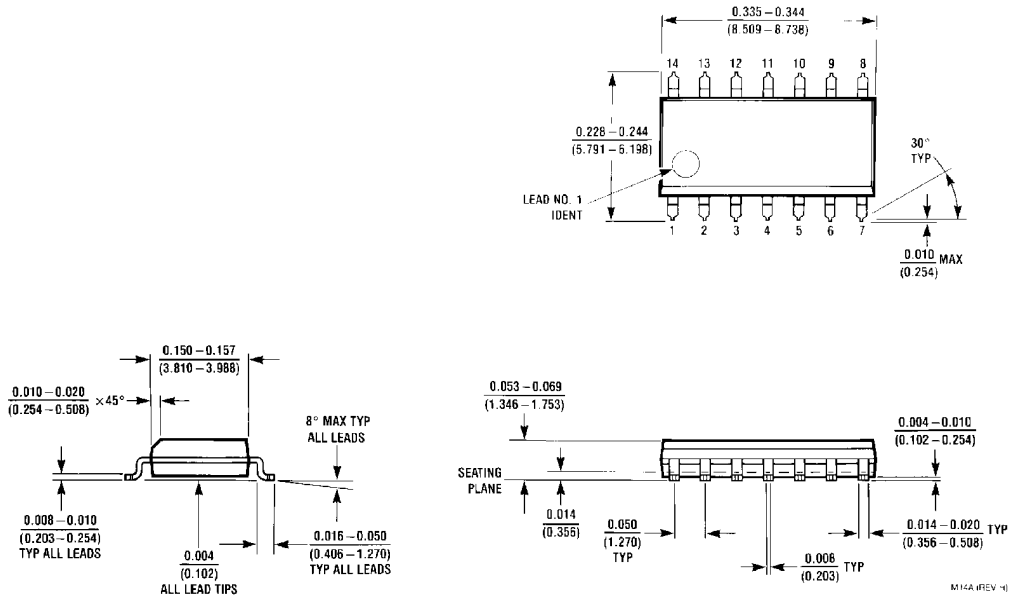
E20A (REV D)

20-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

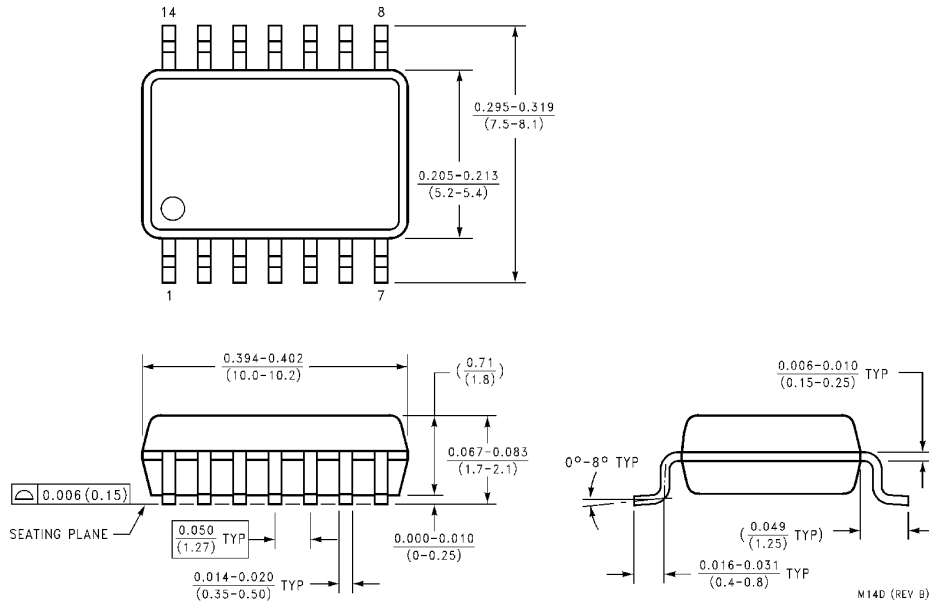


14-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

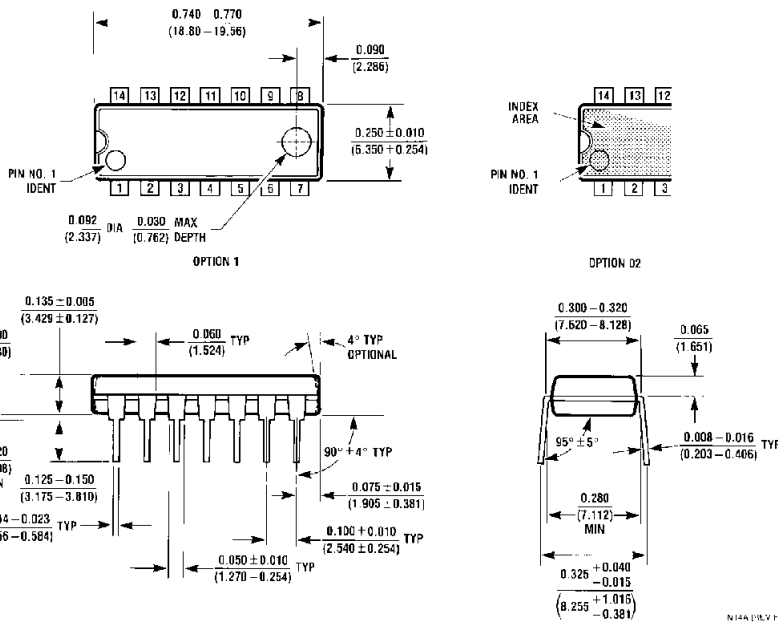


**14-Lead (0.150" Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M14A**

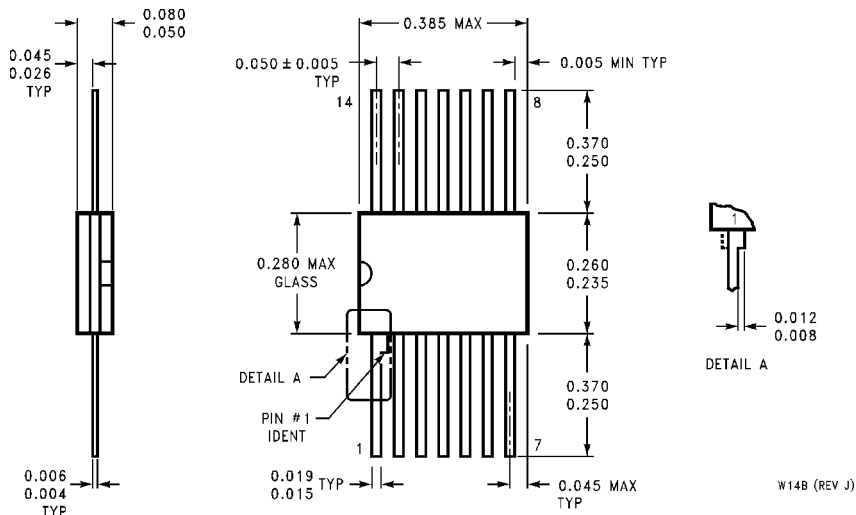


**14-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M14D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**14-Lead (0.300" Wide) (Molded Dual-In-Line Package (P)
NS Package Number N14A**



**14-Lead Ceramic Flatpak (F)
NS Package Number W14B**

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