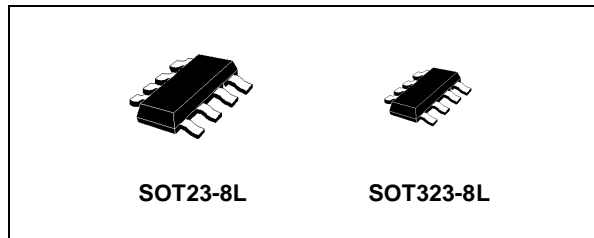




## SINGLE D-TYPE FLIP FLOP WITH PRESET AND CLEAR

### PRELIMINARY DATA

- HIGH SPEED:  
 $f_{MAX} = 170 \text{ MHz (TYP.) at } V_{CC} = 5V$
- LOW POWER DISSIPATION:  
 $I_{CC} = 1\mu\text{A (MAX.) at } T_A = 25^\circ\text{C}$
- COMPATIBLE WITH TTL OUTPUTS:  
 $V_{IH} = 2V \text{ (MIN)}, V_{IL} = 0.8V \text{ (MAX)}$
- POWER DOWN PROTECTION ON INPUTS  
 SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 8\text{mA (MIN)}$
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:  
 $V_{CC(OPR)} = 4.5V \text{ to } 5.5V$
- IMPROVED LATCH-UP IMMUNITY



### ORDER CODES

PACKAGE	T & R
SOT23-8L	74V2T70STR
SOT323-8L	74V2T70CTR

### DESCRIPTION

The 74V2T74 is an advanced high-speed CMOS SINGLE D-TYPE FLIP FLOP WITH PRESET AND CLEAR fabricated with sub-micron silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

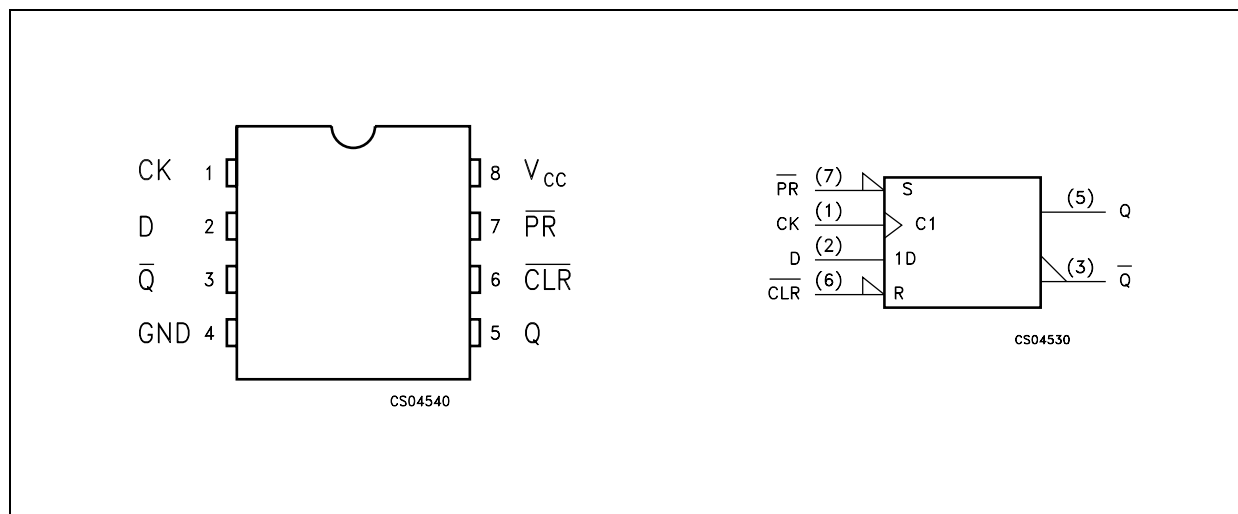
A signal on the D INPUT is transferred to the Q and  $\bar{Q}$  OUTPUTS during the positive going transition of the clock pulse.

CLEAR and PRESET are independent of the clock and accomplished by a low setting on the appropriate input.

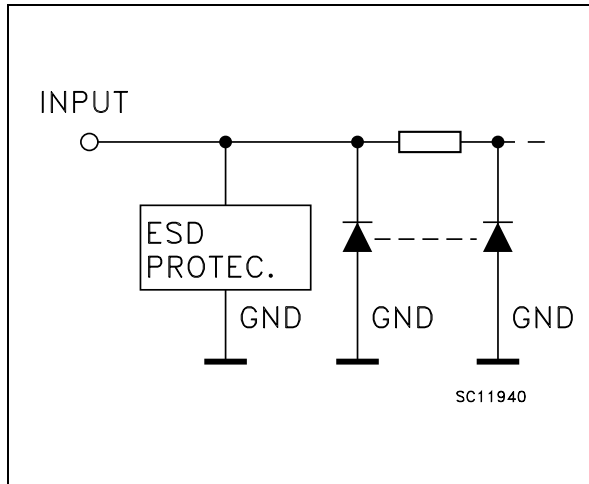
Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V.

All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

### PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

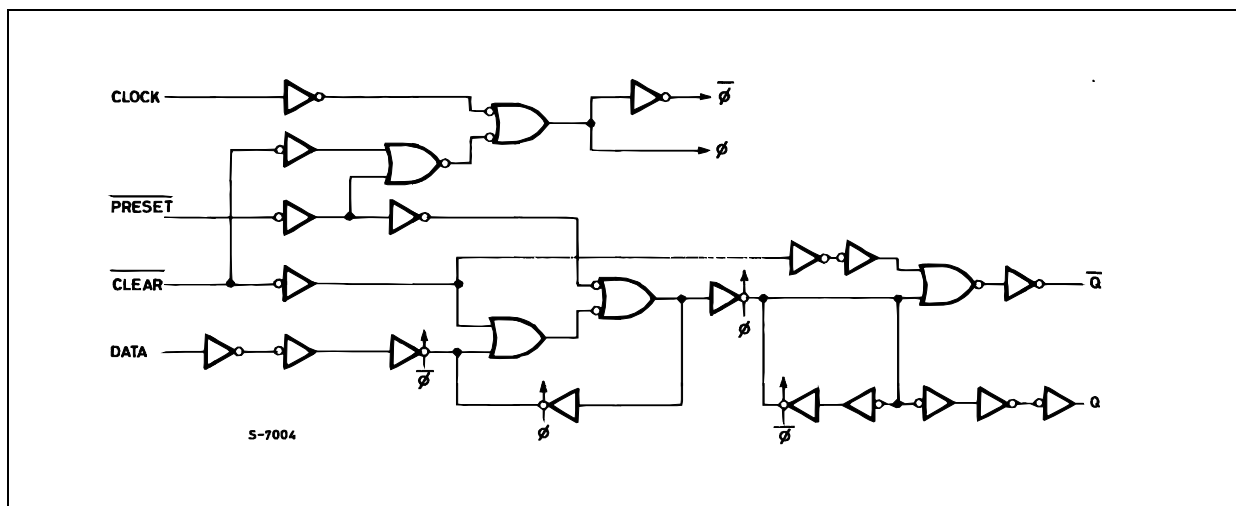
PIN No	SYMBOL	NAME AND FUNCTION
6	$\overline{\text{CLR}}$	Asynchronous Reset - Direct Input
2	D	Data Input
1	CK	Clock Input (LOW to HIGH, Edge Triggered)
7	PR	Asynchronous Set - Direct Input
5	Q	True Flip-Flop Output
3	$\overline{\text{Q}}$	Complement Flip-Flop Output
4	GND	Ground (0V)
8	V <sub>CC</sub>	Positive Supply Voltage

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{\text{CLR}}$	$\overline{\text{PR}}$	D	CK	Q	$\overline{\text{Q}}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	
H	H	L		L	H	
H	H	H		H	L	
H	H	X		Q <sub>n</sub>	$\overline{\text{Q}}_n$	NO CHANGE

X= Don't care

LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to +7.0	V
$V_I$	DC Input Voltage	-0.5 to +7.0	V
$V_O$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	- 20	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Current	$\pm 25$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 50$	mA
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	4.5 to 5.5	V
$V_I$	Input Voltage	0 to 5.5	V
$V_O$	Output Voltage	0 to 5.5	V
$V_O$	Output Voltage	0 to $V_{CC}$	V
$T_{op}$	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (note 1) ( $V_{CC} = 5.0 \pm 0.5V$ )	0 to 20	ns/V

1)  $V_{IN}$  from 0.8V to 2V

## DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V <sub>IH</sub>	High Level Input Voltage	4.5 to 5.5		2			2		2		V
V <sub>IL</sub>	Low Level Input Voltage	4.5 to 5.5				0.8		0.8		0.8	V
V <sub>OH</sub>	High Level Output Voltage	4.5	I <sub>O</sub> =-50 μA	4.4	4.5		4.4		4.4		V
		4.5	I <sub>O</sub> =-8 mA	3.94			3.8		3.7		
V <sub>OL</sub>	Low Level Output Voltage	4.5	I <sub>O</sub> =50 μA		0.0	0.1		0.1		0.1	V
		4.5	I <sub>O</sub> =8 mA			0.36		0.44		0.55	
I <sub>I</sub>	Input Leakage Current	0 to 5.5	V <sub>I</sub> = 5.5V or GND			± 0.1		± 1.0		± 1.0	μA
I <sub>CC</sub>	Quiescent Supply Current	5.5	V <sub>I</sub> = V <sub>CC</sub> or GND			1		10		20	μA
Δ I <sub>CC</sub>	Additional Worst Case Supply Current	5.5	One Input at 3.4V, other input at V <sub>CC</sub> or GND			1.35		1.5		1.5	mA
I <sub>OPD</sub>	Output Leakage Current	0	V <sub>OUT</sub> = 5.5V			0.5		5.0		5.0	μA

AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3ns)

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time CK to Q or $\bar{Q}$	5.0(*)	15		4.6	7.3	1.0	8.5	1.0	8.5	ns
		5.0(*)	50		6.1	9.3	1.0	10.5	1.0	10.5	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time $\overline{PR}$ or $\overline{CLR}$ to Q or $\bar{Q}$	5.0(*)	15		4.8	7.7	1.0	9.0	1.0	9.0	ns
		5.0(*)	50		6.3	9.7	1.0	11.0	1.0	11.0	
t <sub>W</sub>	CK Pulse Width HIGH or LOW	5.0(*)			5.0			5.0		5.0	ns
t <sub>W</sub>	$\overline{PR}$ or $\overline{CLR}$ Pulse Width LOW	5.0(*)			5.0			5.0		5.0	ns
t <sub>s</sub>	Setup Time D to CK HIGH or LOW	5.0(*)			5.0			5.0		5.0	ns
t <sub>h</sub>	Hold Time D to CK HIGH or LOW	5.0(*)			0.5			0.5		0.5	ns
t <sub>REM</sub>	Removal Time $\overline{PR}$ or $\overline{CLR}$ to CK	5.0(*)			3.0			3.0		3.0	ns
f <sub>MAX</sub>	Maximum Clock Frequency	5.0(*)	15		100	160		80		80	MHz
		5.0(*)	50		80	140		65		65	

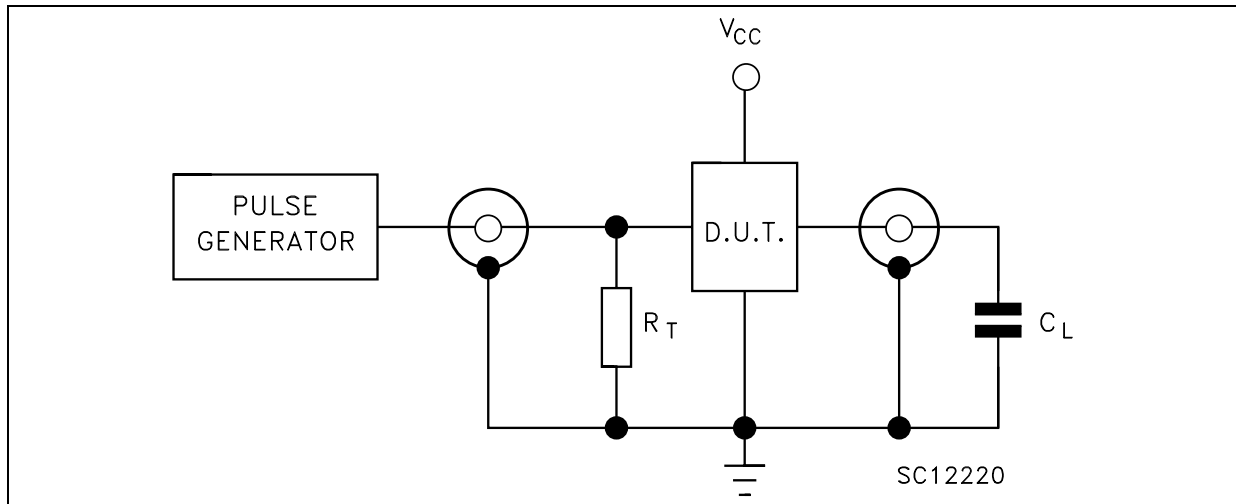
(\*) Voltage range is 5.0V ± 0.5V

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C <sub>IN</sub>	Input Capacitance	5.0			4	10		10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (note 1)	5.0	f <sub>IN</sub> = 10MHz		22						pF

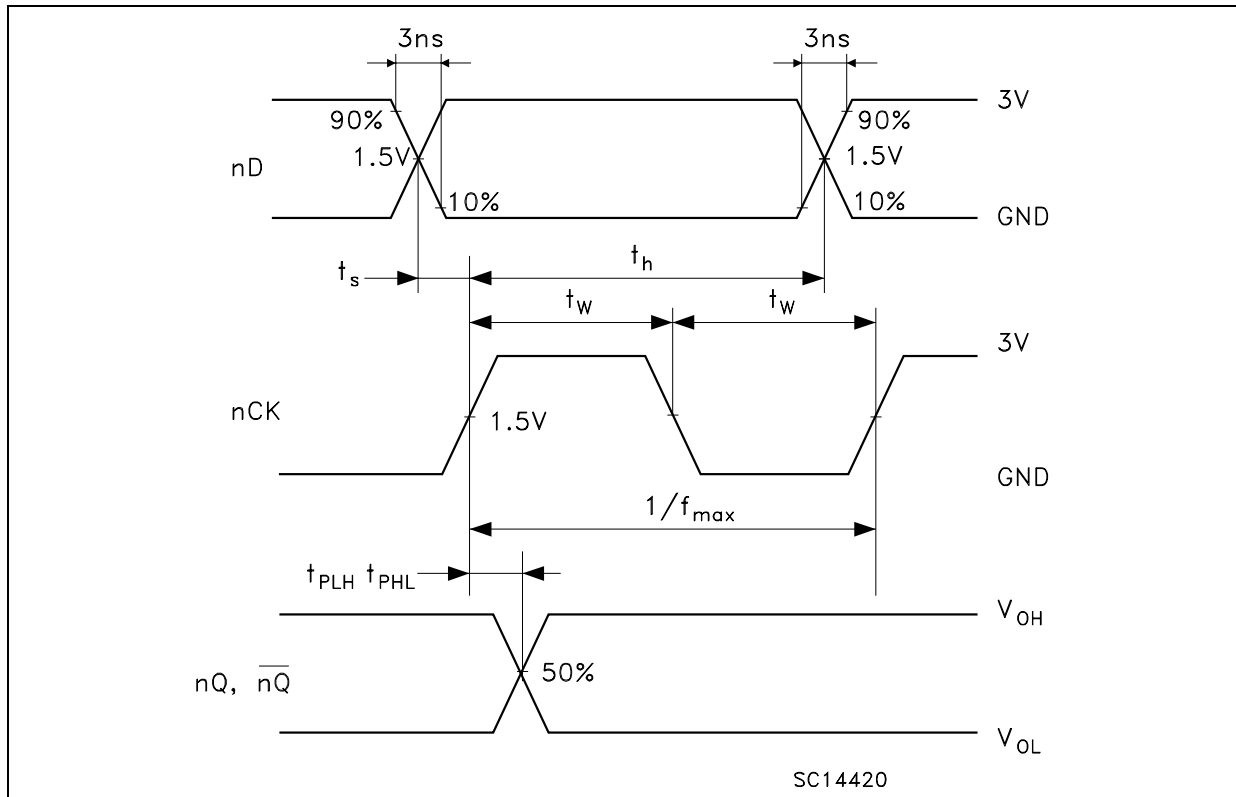
1) C<sub>PD</sub> is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

## TEST CIRCUIT

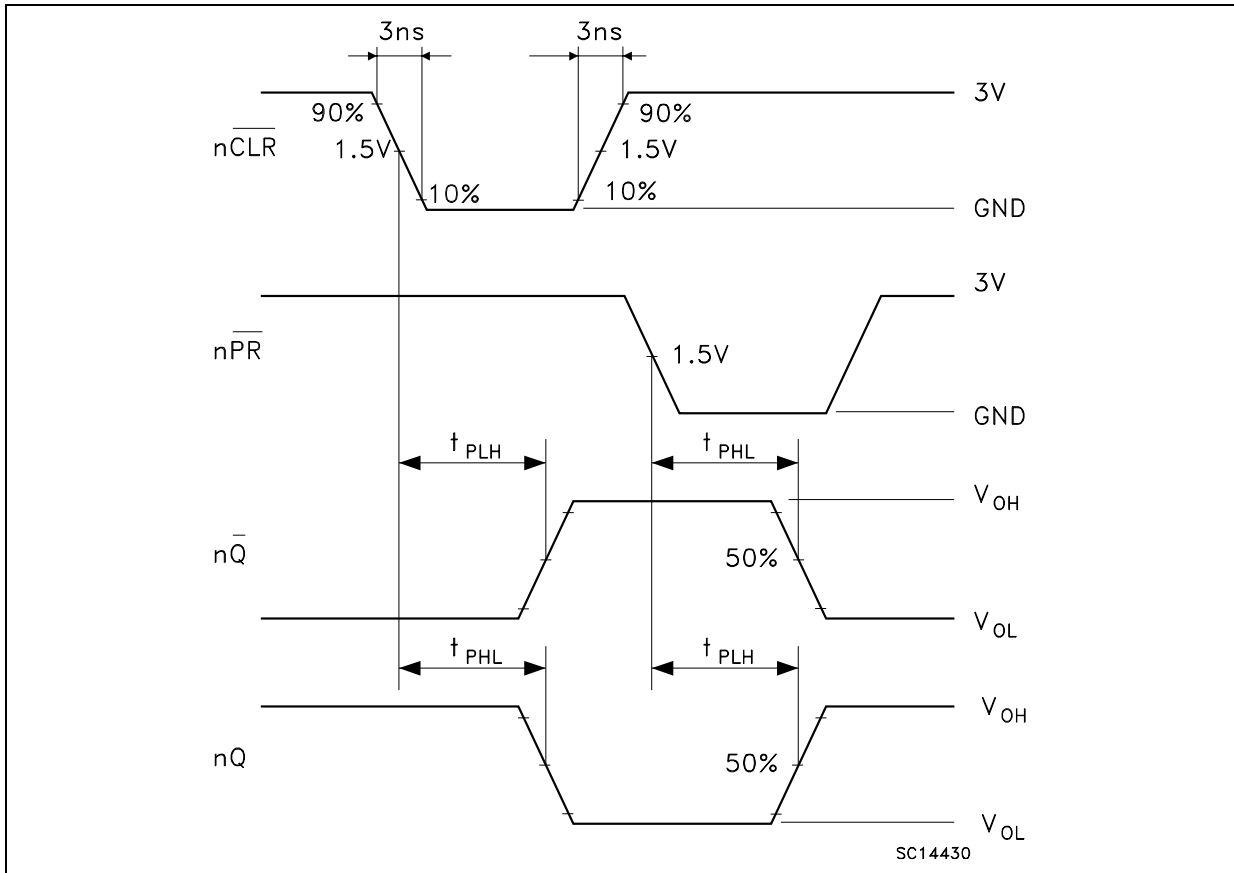


C<sub>L</sub> = 15/50pF or equivalent (includes jig and probe capacitance)  
R<sub>T</sub> = Z<sub>OUT</sub> of pulse generator (typically 50Ω)

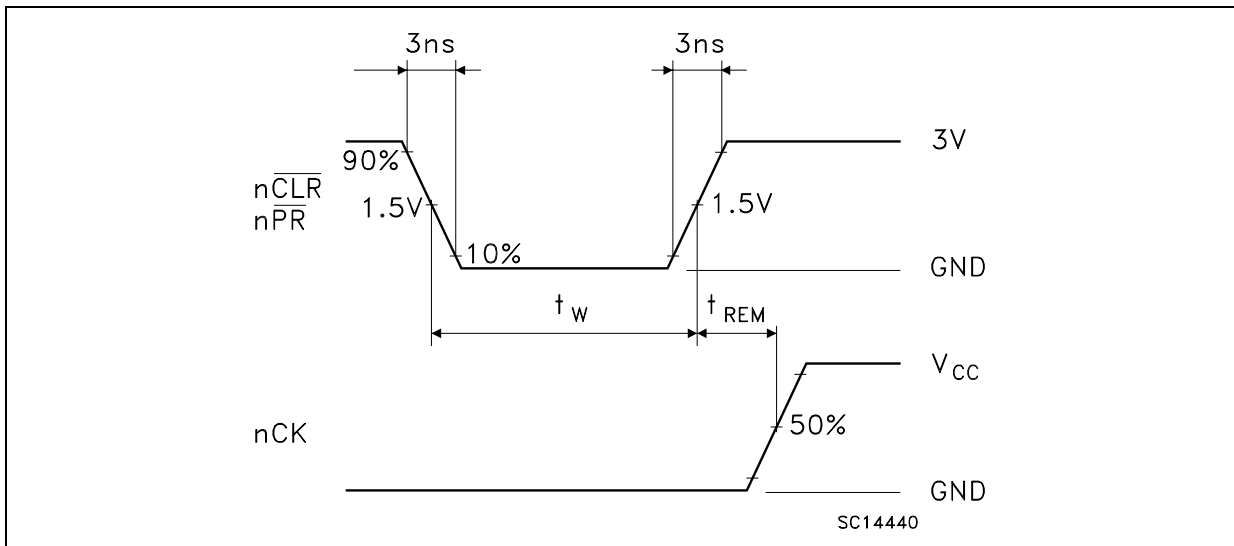
**WAVEFORM 1: PROPAGATION DELAYS, SETUP AND HOLD TIMES (D TO CK), CK MAXIMUM FREQUENCY , CK MINIMUM PULSE WIDTH (f=1MHz; 50% duty cycle)**



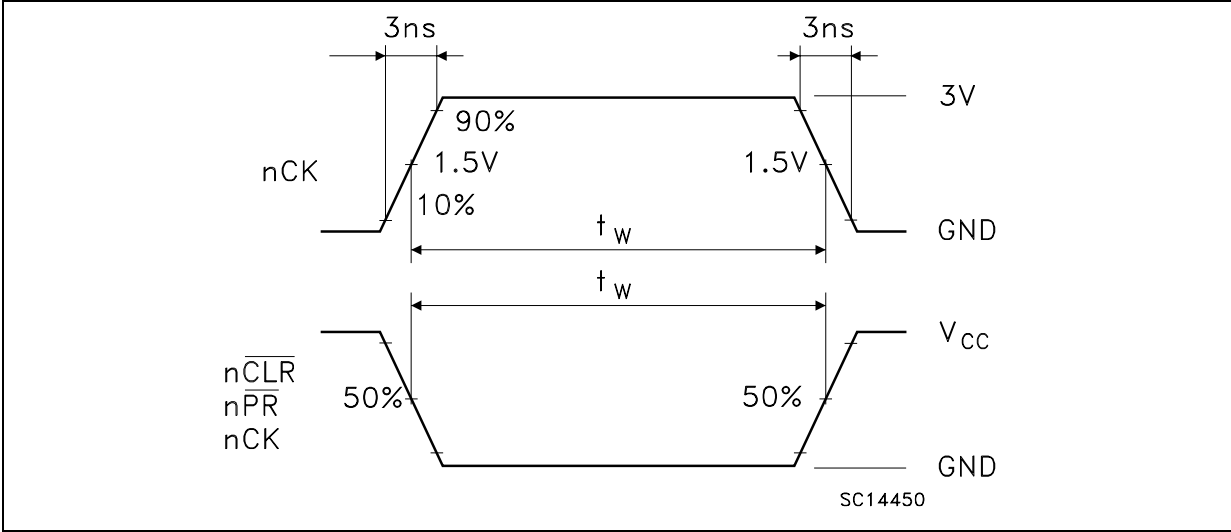
**WAVEFORM 2: PROPAGATION DELAYS, MINIMUM PULSEWIDTH (f=1MHz; 50% duty cycle)**



**WAVEFORM 3: REMOVAL TIME (f=1MHz; 50% duty cycle)**



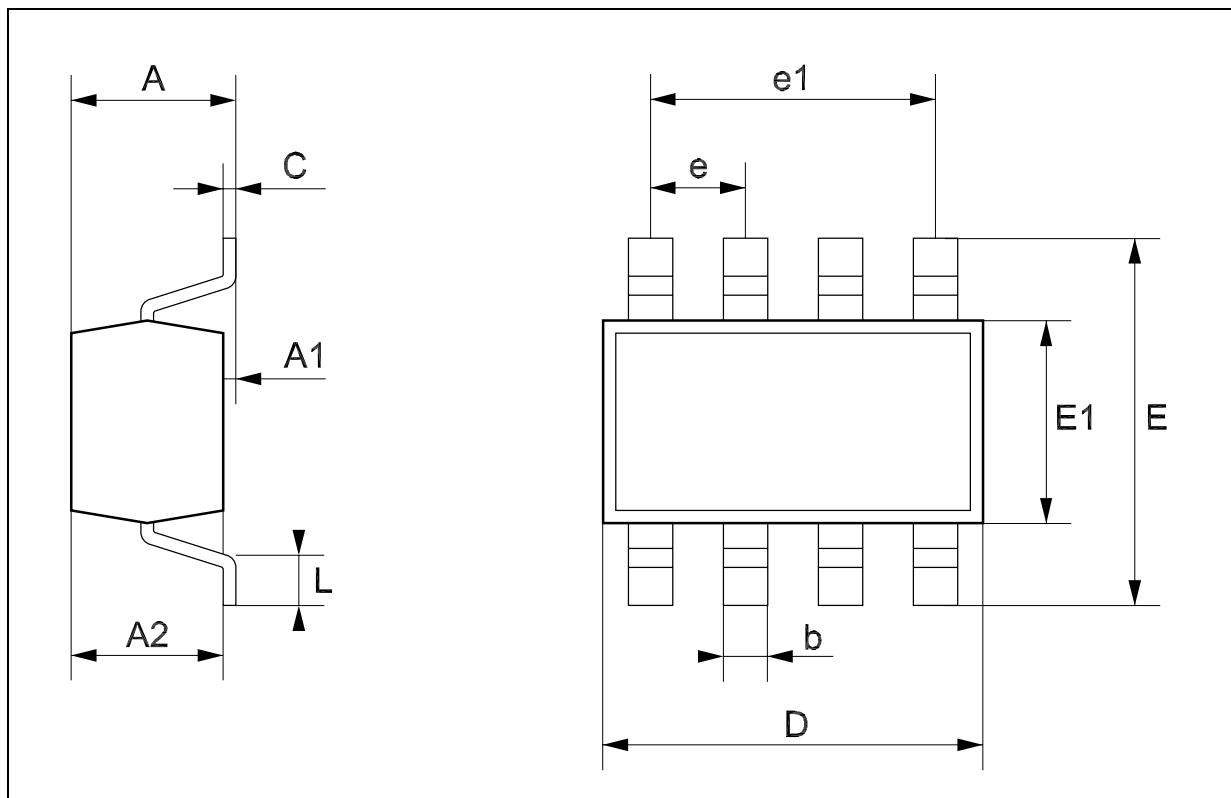
WAVEFORM 4: PULSE WIDTHS





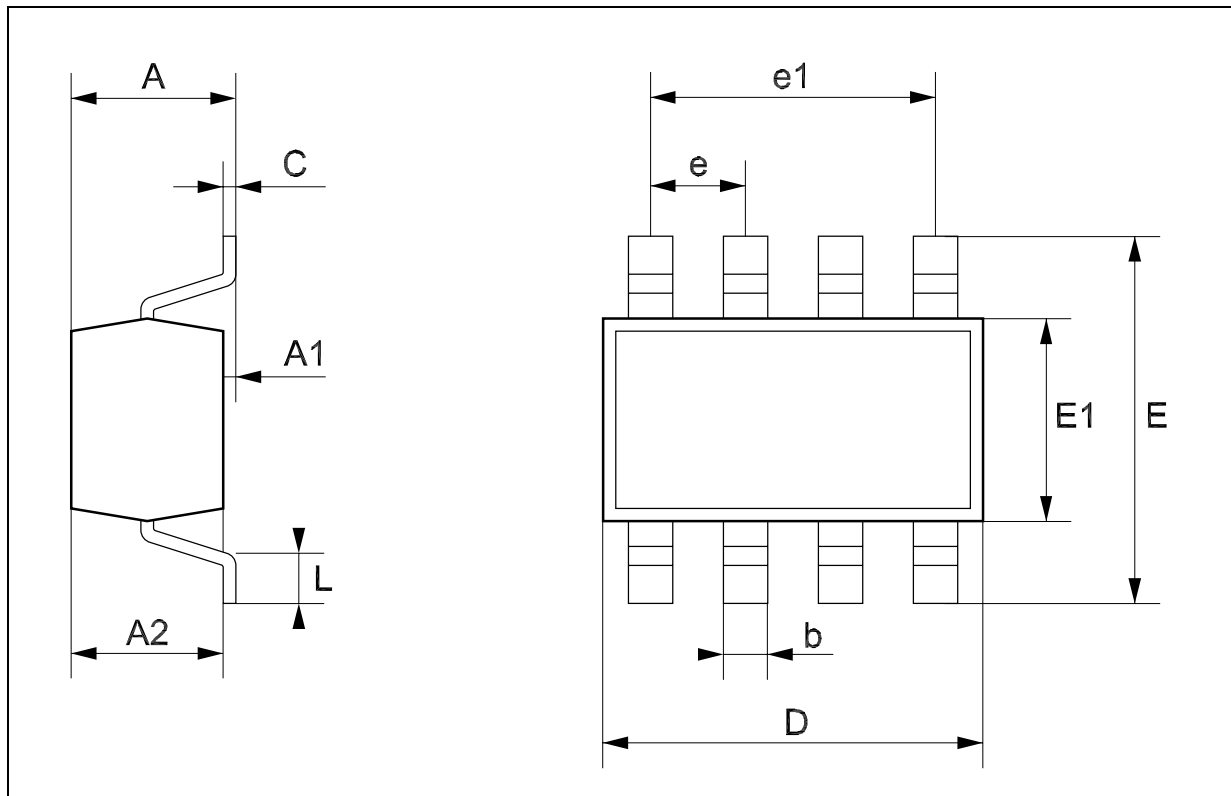
<b>SOT23-8L MECHANICAL DATA</b>
---------------------------------

DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.90		1.45	35.4		57.1
A1	0.00		0.15	0.0		5.9
A2	0.90		1.30	35.4		51.2
b	0.22		0.38	8.6		14.9
C	0.09		0.20	3.5		7.8
D	2.80		3.00	110.2		118.1
E	2.60		3.00	102.3		118.1
E1	1.50		1.75	59.0		68.8
e	0	.65			25.6	
e1		1.95			76.7	
L	0.35		0.55	13.7		21.6



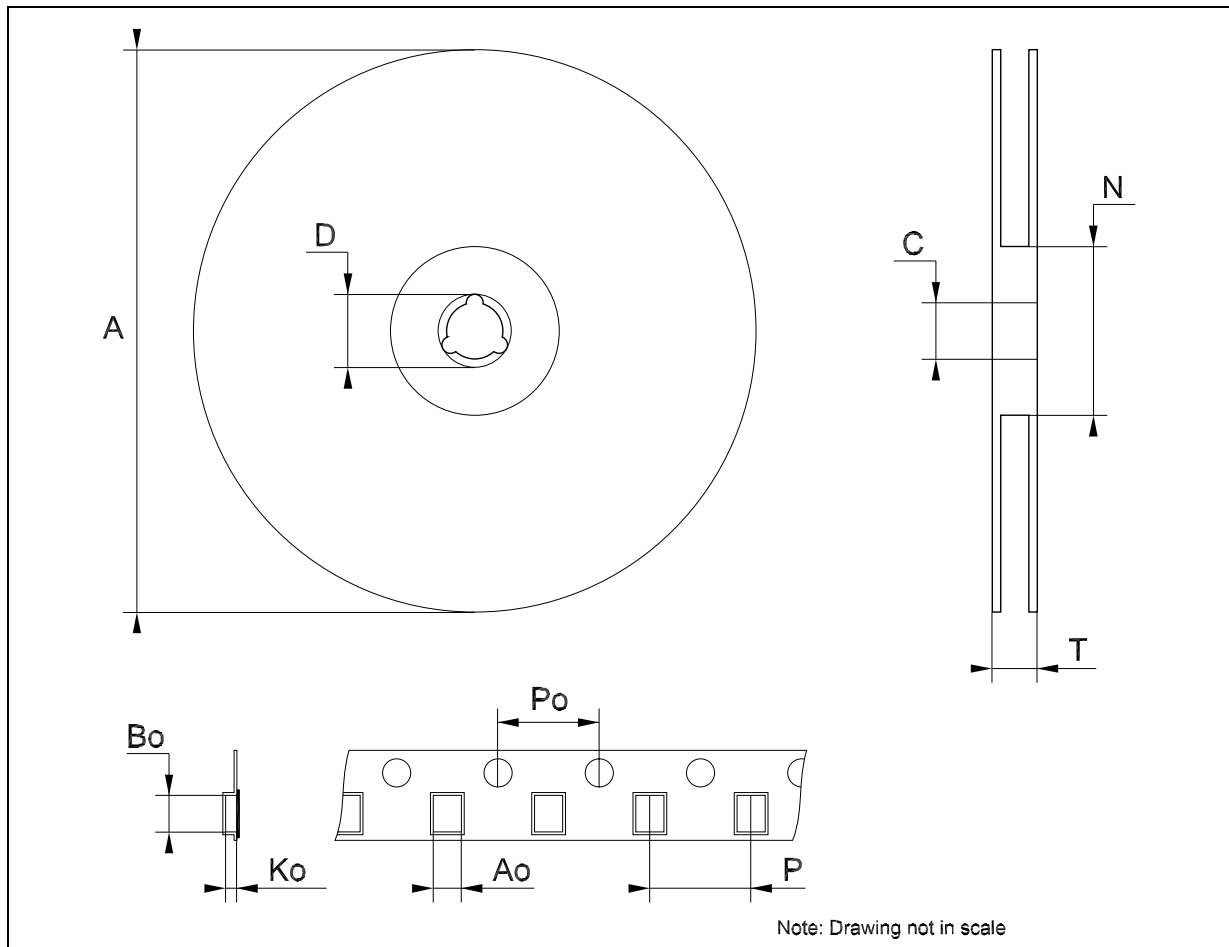
## SOT323-8L MECHANICAL DATA

DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80		1.10	31.5		43.3
A1	0.00		0.10	0.0		3.9
A2	0.80		1.00	31.5		34.9
b	0.13		0.28	5.1		11.0
C	0.10		0.18	3.9		7.1
D	1.80		2.20	70.9		86.6
E	1.80		2.40	70.9		94.5
E1	1.15		1.35	45.3		53.1
e		0.5			19.7	
e1		1.5			59.0	
L	0.10		0.30	3.9		11.8



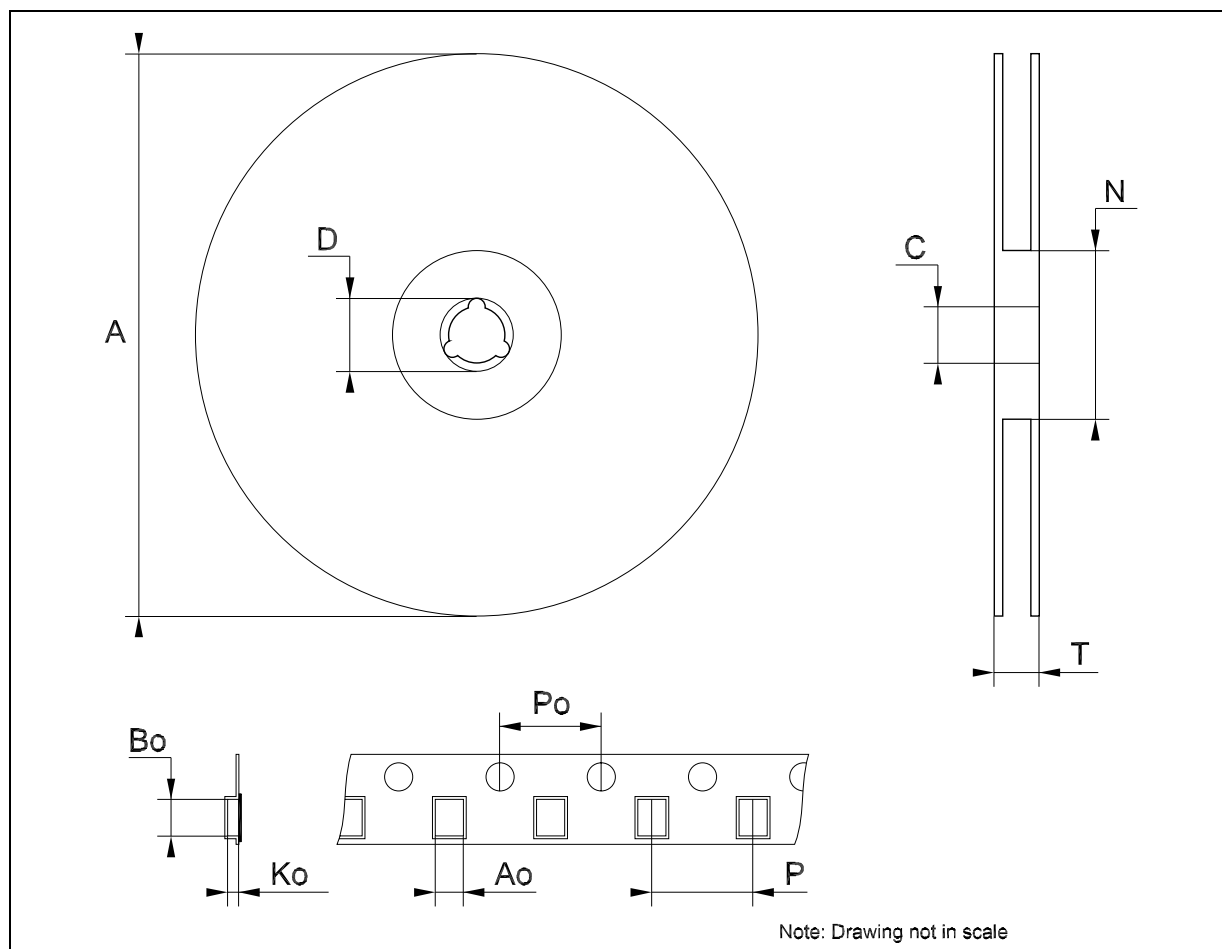
### Tape & Reel SOT23-xL MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			180			7.086
C	12.8	13.0	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao	3.13	3.23	3.33	0.123	0.127	0.131
Bo	3.07	3.17	3.27	0.120	0.124	0.128
Ko	1.27	1.37	1.47	0.050	0.054	0.058
Po	3.9	4.0	4.1	0.153	0.157	0.161
P	3.9	4.0	4.1	0.153	0.157	0.161



## Tape &amp; Reel SOT323-xL MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	175	180	185	6.889	7.086	7.283
C	12.8	13	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	59.5	60	60.5		2.362	
T			14.4			0.567
Ao		2.25			0.088	
Bo		2.7			0.106	
Ko		1.2			0.047	
Po	3.98	4	4.2	0.156	0.157	0.165
P	3.98	4	4.2	0.156	0.157	0.165



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2001 STMicroelectronics - Printed in Italy - All Rights Reserved  
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco  
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© <http://www.st.com>

